BK7236 Datasheet

DS-BK7236-E12 V2.0

2025/6/16

Contents

1. Features

Wi-Fi®

- IEEE 802.11b/g/n/ax 1x1 compliant
- 20 MHz and 40 MHz channel bandwidths for 2.4 GHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports Orthogonal Frequency Division Multiple Access (OFDMA)
- Supports Target Wake Time (TWT)
- TX and RX Low-Density Parity Check (LDPC) support for extended range
- WPA™/WPA2™/WPA3™-Personal support for enhanced security
- Supports STA and SoftAP modes
- Supports concurrent SoftAP + STA
- TX power up to +21 dBm
- RX sensitivity -98 dBm

Bluetooth® Low Energy

- Bluetooth Low Energy (LE) 5.4
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: LE Audio, Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, 2 Mbps, advertising extensions, and long range
- Supports an antenna array with up to 16 antennas for precise positioning

Core

- Arm®v8-M STAR-MC1 MCU at up to 320 MHz:
  - Double-precision floating-point unit (FPU)
  - 16 KB ITCM + 16 KB DTCM
  - Embedded TrustZone®
  - Supports DSP instructions with SIMD
  - 3.84 CoreMark®/MHz
- UART flash download
- Serial Wire Debug (SWD) interface

Memories

- Flash (XIP): SiP flash up to 8 MB, external flash up to 16 MB
- SiP PSRAM: up to 16 MB
- 640 KB Share SRAM
- 64 KB ROM
- eFuse

Security

The BK7236 integrates the IoT Platform Security Suite (IPSS) for cryptograph and system security control. The key features of the IPSS include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine, which includes the following features:
  - Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
  - Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
  - Digest schemes, SHA1/224/256
  - Digest scheme, SM3
  - Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
  - Asymmetric scheme, SM2
  - Key ladder for key management
  - Lifecycle management
  - True random number generator

Clock Management

- External oscillators: 26 MHz crystal oscillator (XTALH), 32 kHz crystal oscillator (XTALL) (BK7236QH4150 only)
- Internal oscillators: 26–360 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 320 MHz/480 MHz PLL (DPLL)

- Audio PLL (APLL)

Power Management

- 2.0 to 4.35 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converters and LDO regulators
- Low power consumption:
  - Active mode RX: 17.5 mA
  - Sleep mode: 43 μA
  - Deep sleep mode: 16 μA
  - Shutdown mode: 2.5 μA

Peripherals

- GPIOs: 21 in BK7236QH4068/BK7236QH4050 QFN40, 19 in BK7236QH4150 QFN40
- 1x SPI
- 3x UART, 1 with hardware flow control and flash download support
- 1x SDIO
- 1x I2C
- 1x high-speed USB2.0 (HS) (BK7236QH4150 only)
- 1x LIN controller
- 2x general-purpose DMA controller (GDMA), each with 8 channels
- 9x 32-bit PWM channel
- 1x DMIC (BK7236QH4150 only)
- 12-bit AUX ADC, up to 8 channels
- 6x 32-bit general-purpose timer
- 2x watchdog timer
- 1x real-time counter (RTC)
- 1x IrDA interface (BK7236QH4068/BK7236QH4050 only)
- 1x temperature sensor
- 1x touch sensor (TOUCH), 6 touch sensing I/Os

Packaging

- BK7236QH4068: QFN40 package, 5 x 5 x 0.9 mm
- BK7236QH4050/BK7236QH4150: QFN40 package, 5 x 5 x 0.75 mm

- Operating temperature range: -40 to +105 °C

Applications

- Home appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart plug
- Smart lighting
  - Light bulb
  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

2. Overview

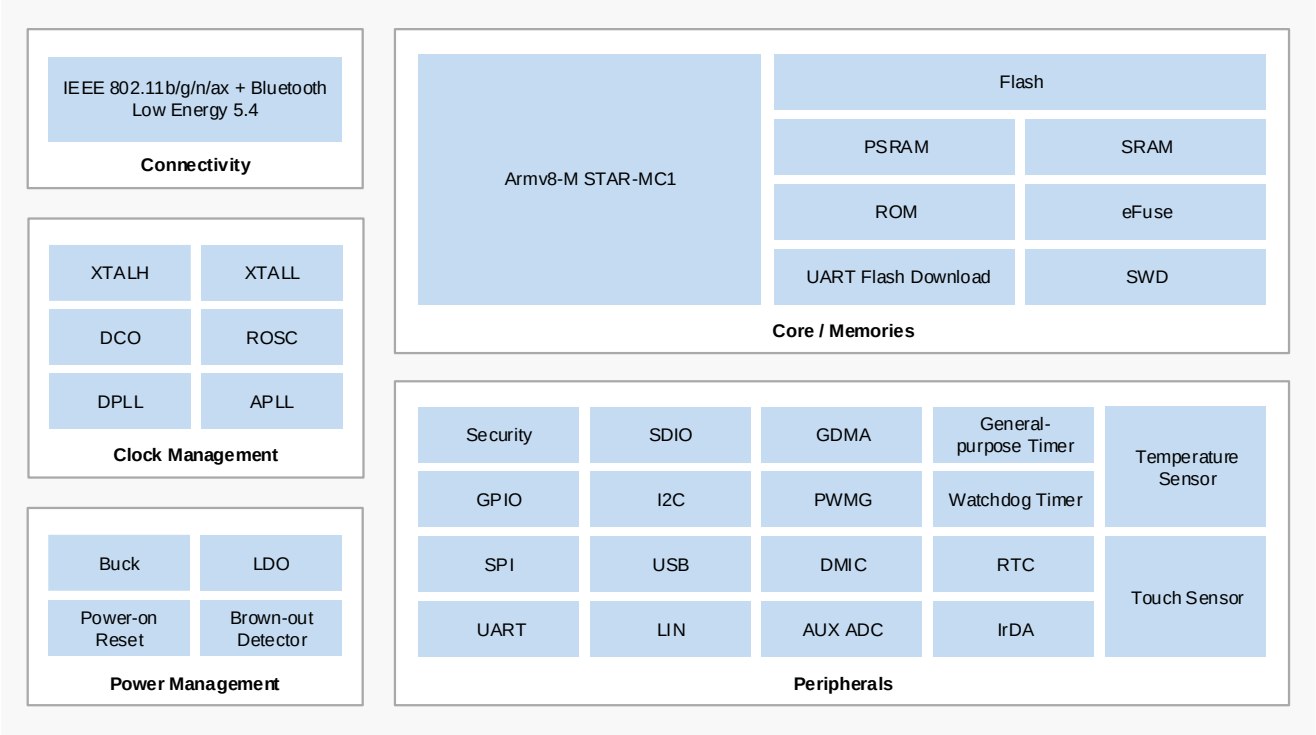
The BK7236 is a highly integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and Bluetooth Low Energy (LE) 5.4 combo solution designed for applications that require high security and abundant resources. The integration of a 32-bit Armv8-M STAR-MC1 MCU and a comprehensive set of peripherals makes the BK7236 ideal for advanced Internet of Things (IoT) applications.

The BK7236 provides state-of-the-art security based on a powerful security architecture. The BK7236 integrates an IoT Platform Security Suite (IPSS) for cryptograph and system security control. The IPSS embeds all-round and robust security features to set up a top-secret execution environment for IoT devices.

Using advanced design techniques and ultra-low power process technology, the BK7236 delivers high integration, efficient security, and minimal power consumption for a wide range of advanced IoT applications.

Figure 2-1 shows the general block diagram of the BK7236.

Figure 2-1 BK7236 Block Diagram



The BK7236 devices are offered in QFN40 packages. The BK7236QH4068, BK7236QH4050, and BK7236QH4150 each come in a QFN40 package. The BK7236QH4068 and BK7236QH4050 have the same pin assignments, while the BK7236QH4150's pin assignments are different. The set of included peripherals varies depending on the package. Table 2-1 shows the list of peripherals available on each package.

Table 2-1 Device Options and Features

Feature		BK7236QH4068 QFN40	BK7236QH4050 QFN40	BK7236QH4150 QFN40
Flash		8 MB	4 MB	4 MB
PSRAM		8 MB	-	-
GPIO		21	21	19
SPI	Master/Slave	1	1	1
UART		3	3	3 (hardware flow control unavailable for UART0)
SDIO		1	1	1
I2C	Master/Slave	1	1	1
USB		-	-	1
LIN		1	1	1
GDMA		2	2	2
PWM	PWM0–11	7 (PWMG0_PWM0/1/4/5, PWMG1_0/2/4)	7 (PWMG0_PWM0/1/4/5, PWMG1_0/2/4)	8 (PWMG0_PWM0/1/2/3/4, PWMG1_0/2/4)
DMIC		-	-	1
AUX ADC	12 bits	1	1	1
	Number of channels	7 (ADC1/2/4/12/13/14/15)	7 (ADC1/2/4/12/13/14/15)	5 (ADC2/4/10/12/13)
General-purpose timer		6	6	6
Watchdog timer (WDT)		2	2	2
Real-time counter (RTC)		1	1	1
IrDA		1	1	-
Temperature sensor		1	1	1
Touch sensing I/O		6 (TOUCH0/1/2/6/8/10)	6 (TOUCH0/1/2/6/8/10)	4 (TOUCH2/6/8/10)
Package		5 x 5 x 0.9 mm QFN40	5 x 5 x 0.75 mm QFN40	5 x 5 x 0.75 mm QFN40
Operating voltage		2.0 to 4.35 V		
Operating temperature		-40 to +105 °C		

3. Pin Descriptions

The BK7236 provides Wi-Fi and Bluetooth LE functionality in 5 x 5 mm, 40-pin QFN packages.

3.1 BK7236QH4068/50 QFN40 Pin Descriptions

Figure 3-1 shows the pin assignments of the QFN40 package for BK7236QH4068 and BK7236QH4050.

Figure 3-1 BK7236QH4068/50 QFN40 Pin Assignments

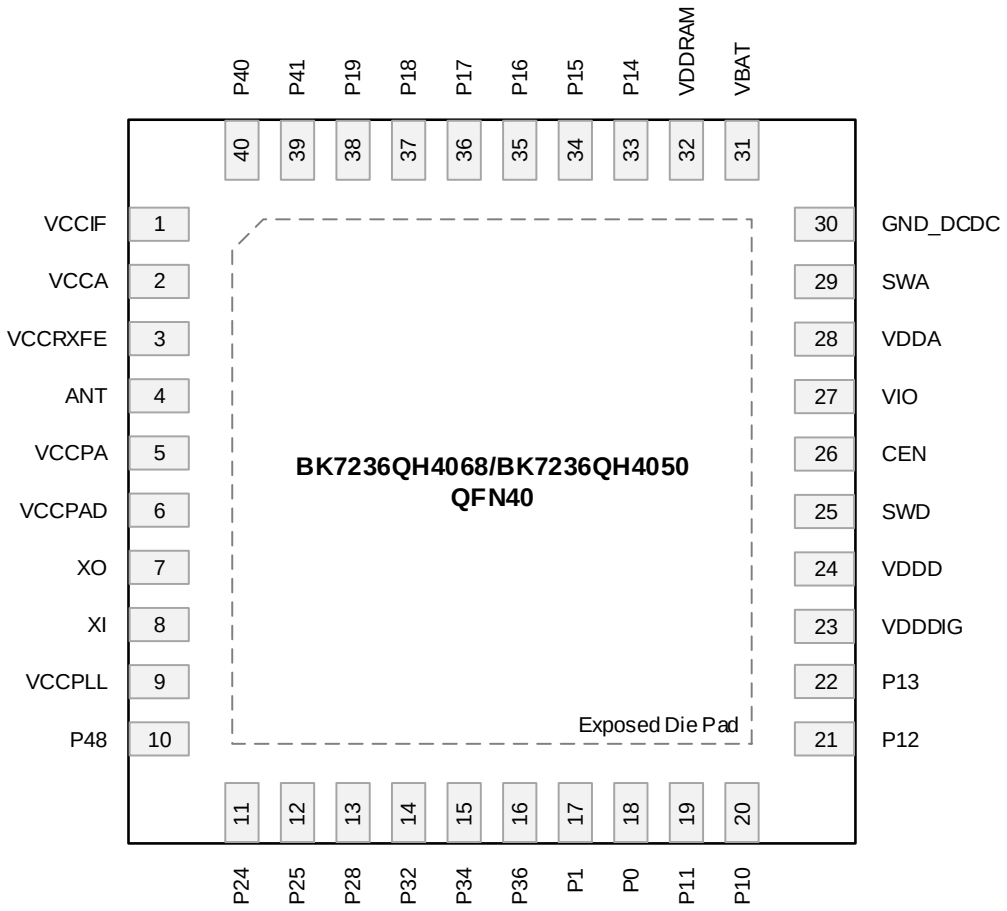


Table 3-1 shows the pin descriptions of the QFN40 package for BK7236QH4068 and BK7236QH4050.

Table 3-1 BK7236QH4068/50 QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCIF	-	Analog input	IF power supply

Pin #	Name	I/O	Type	Description
2	VCCA	-	Analog input	Analog power supply
3	VCCRXFE	-	Analog input	RF receiver power supply
4	ANT	-	RF	2.4 GHz RF signal port
5	VCCPA	-	Analog input	RF PA power supply
6	VCCPAD	-	Analog input	RF PA driver power supply
7	XO	-	Analog output	26 MHz crystal output
8	XI	-	Analog input	26 MHz crystal input
9	VCCPLL	-	Analog input	RF PLL power supply
10	P48	I/O	Digital	GPIO48: general-purpose I/O
11	P24	I/O	Digital/Analog	• GPIO24: general-purpose I/O • LPO_CLK: 32 kHz clock output • PWMG0_PWM4: PWM4 channel of PWMG0 • ADC2: analog input channel
12	P25	I/O	Digital/Analog	• GPIO25: general-purpose I/O • IRDA: infrared data • PWMG0_PWM5: PWM5 channel of PWMG0 • ADC1: analog input channel
13	P28	I/O	Digital/Analog	• GPIO28: general-purpose I/O • I2S_MCLK: master clock • ADC4: analog input channel • TOUCH2: touch sensing I/O • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
14	P32	I/O	Digital/Analog	• GPIO32: general-purpose I/O • PWMG1_PWM0: PWM0 channel of PWMG1 • TOUCH6: touch sensing I/O
15	P34	I/O	Digital/Analog	• GPIO34: general-purpose I/O • PWMG1_PWM2: PWM2 channel of PWMG1 • TOUCH8: touch sensing I/O

Pin #	Name	I/O	Type	Description
				• SPI0_CSN: chip select
16	P36	I/O	Digital/Analog	• GPIO36: general-purpose I/O • PWMG1_PWM4: PWM4 channel of PWMG1 • TOUCH10: touch sensing I/O • SPI0_MISO: master in slave out
17	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data • SWDIO: serial wire data • ADC13: analog input channel • LIN_RXD: receive data input
18	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock • SWCLK: serial wire clock • ADC12: analog input channel • LIN_TXD: transmit data output
19	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output • UART0_TX: transmit data output • SDIO_DATA3: data
20	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input • UART0_RX: receive data input • SDIO_DATA2: data • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
21	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • UART0_RTS: request to send • TOUCH0: touch sensing I/O • ADC14: analog input channel
22	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• UART0_CTS: clear to send • TOUCH1: touch sensing I/O • ADC15: analog input channel
23	VDDDIG	-	Analog output	Digital core LDO output
24	VDDD	-	Analog output	Digital buck/LDO output
25	SWD	-	Analog output	Digital buck switch output
26	CEN	-	Analog input	Chip enable, active high
27	VIO	-	Analog output	IO LDO output
28	VDDA	-	Analog output	Analog buck/LDO output
29	SWA	-	Analog output	Analog buck switch output
30	GND_DCDC	-	GND	Buck ground
31	VBAT	-	Power	Chip power supply
32	VDDRAM	-	Analog output	EXMEM LDO output
33	P14	I/O	Digital	• GPIO14: general-purpose I/O • SDIO_CLK: clock • SPI0_SCK: serial clock • BT_ANT0: Bluetooth antenna select • I2C1_SCL: serial clock
34	P15	I/O	Digital	• GPIO15: general-purpose I/O • SDIO_CMD: command/response • SPI0_CSN: chip select • BT_ANT1: Bluetooth antenna select • I2C1_SDA: serial data
35	P16	I/O	Digital	• GPIO16: general-purpose I/O • SDIO_DATA0: data • SPI0_MOSI: master out slave in • BT_ANT2: Bluetooth antenna select
36	P17	I/O	Digital	• GPIO17: general-purpose I/O • SDIO_DATA1: data • SPI0_MISO: master in slave out • BT_ANT3: Bluetooth antenna select
37	P18	I/O	Digital	• GPIO18: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• SDIO_DATA2: data • PWMG0_PWM0: PWM0 channel of PWMG0
38	P19	I/O	Digital/Analog	• GPIO19: general-purpose I/O • SDIO_DATA3: data • PWMG0_PWM1: PWM1 channel of PWMG0
39	P41	I/O	Digital	• GPIO41: general-purpose I/O • UART2_TX: transmit data output • LIN_TXD: transmit data output
40	P40	I/O	Digital	• GPIO40: general-purpose I/O • UART2_RX: receive data input • LIN_RXD: receive data input
Die pad	GND_SLUG	-	GND	Ground

3.2 BK7236QH4150 QFN40 Pin Descriptions

Figure 3-2 shows the pin assignments of the BK7236QH4150 QFN40 package.

Figure 3-2 BK7236QH4150 QFN40 Pin Assignments

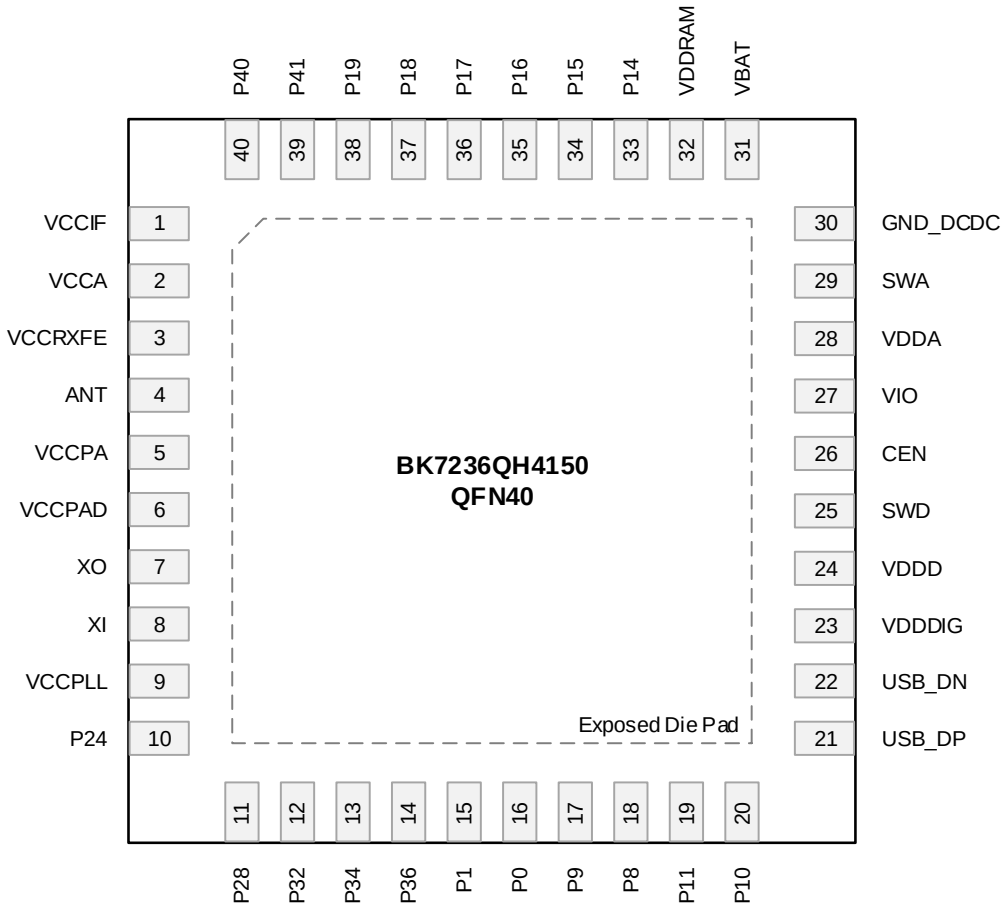


Table 3-2 shows the pin descriptions of the BK7236QH4150 QFN40 package.

Table 3-2 BK7236QH4150 QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCIF	-	Analog input	IF power supply
2	VCCA	-	Analog input	Analog power supply
3	VCCRXFE	-	Analog input	RF receiver power supply
4	ANT	-	RF	2.4 GHz RF signal port
5	VCCPA	-	Analog input	RF PA power supply
6	VCCPAD	-	Analog input	RF PA driver power supply
7	XO	-	Analog output	26 MHz crystal output
8	XI	-	Analog input	26 MHz crystal input

Pin #	Name	I/O	Type	Description
9	VCCPLL	-	Analog input	RF PLL power supply
10	P24	I/O	Digital/Analog	• GPIO24: general-purpose I/O • LPO_CLK: 32 kHz clock output • PWMG0_PWM4: PWM4 channel of PWMG0 • ADC2: analog input channel
11	P28	I/O	Digital/Analog	• GPIO28: general-purpose I/O • I2S_MCLK: master clock • ADC4: analog input channel • TOUCH2: touch sensing I/O • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
12	P32	I/O	Digital/Analog	• GPIO32: general-purpose I/O • PWMG1_PWM0: PWM0 channel of PWMG1 • TOUCH6: touch sensing I/O
13	P34	I/O	Digital/Analog	• GPIO34: general-purpose I/O • PWMG1_PWM2: PWM2 channel of PWMG1 • TOUCH8: touch sensing I/O • SPI0_CSN: chip select
14	P36	I/O	Digital/Analog	• GPIO36: general-purpose I/O • PWMG1_PWM4: PWM4 channel of PWMG1 • TOUCH10: touch sensing I/O • SPI0_MISO: master in slave out
15	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data • SWDIO: serial wire data • ADC13: analog input channel • LIN_RXD: receive data input
16	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock

Pin #	Name	I/O	Type	Description
				• SWCLK: serial wire clock • ADC12: analog input channel • LIN_TXD: transmit data output
17	P9	I/O	Digital/Analog	• GPIO9: general-purpose I/O • PWMG0_PWM3: PWM3 channel of PWMG0 • DMIC_DAT: data • 32K_XI: 32.768 kHz crystal input
18	P8	I/O	Digital/Analog	• GPIO8: general-purpose I/O • PWMG0_PWM2: PWM2 channel of PWMG0 • DMIC_CLK: clock • ADC10: analog input channel • 32K_XO: 32.768 kHz crystal output
19	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output • UART0_TX: transmit data output • SDIO_DATA3: data
20	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input • UART0_RX: receive data input • SDIO_DATA2: data • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
21	USB_DP	I/O	Digital	USB D+
22	USB_DN	I/O	Digital	USB D-
23	VDDDIG	-	Analog output	Digital core LDO output
24	VDDD	-	Analog output	Digital buck/LDO output
25	SWD	-	Analog output	Digital buck switch output
26	CEN	-	Analog input	Chip enable, active high
27	VIO	-	Analog output	IO LDO output

Pin #	Name	I/O	Type	Description
28	VDDA	-	Analog output	Analog buck/LDO output
29	SWA	-	Analog output	Analog buck switch output
30	GND_DCDC	-	GND	Buck ground
31	VBAT	-	Power	Chip power supply
32	VDDRAM	-	Analog output	EXMEM LDO output
33	P14	I/O	Digital	• GPIO14: general-purpose I/O • SDIO_CLK: clock • SPI0_SCK: serial clock • BT_ANT0: Bluetooth antenna select • I2C1_SCL: serial clock
34	P15	I/O	Digital	• GPIO15: general-purpose I/O • SDIO_CMD: command/response • SPI0_CSN: chip select • BT_ANT1: Bluetooth antenna select • I2C1_SDA: serial data
35	P16	I/O	Digital	• GPIO16: general-purpose I/O • SDIO_DATA0: data • SPI0_MOSI: master out slave in • BT_ANT2: Bluetooth antenna select
36	P17	I/O	Digital	• GPIO17: general-purpose I/O • SDIO_DATA1: data • SPI0_MISO: master in slave out • BT_ANT3: Bluetooth antenna select
37	P18	I/O	Digital	• GPIO18: general-purpose I/O • SDIO_DATA2: data • PWMG0_PWM0: PWM0 channel of PWMG0
38	P19	I/O	Digital	• GPIO19: general-purpose I/O • SDIO_DATA3: data • PWMG0_PWM1: PWM1 channel of PWMG0
39	P41	I/O	Digital	• GPIO41: general-purpose I/O • UART2_TX: transmit data output

Pin #	Name	I/O	Type	Description
				• LIN_TXD: transmit data output
40	P40	I/O	Digital	• GPIO40: general-purpose I/O • UART2_RX: receive data input • LIN_RXD: receive data input
Die pad	GND_SLUG	-	GND	Ground

3.3 Pin Multiplexing

Table 3-3 shows the pin mux functions of GPIOs.

Table 3-3 Pin Multiplexing

GPIO	Flash Download	Alternate Functions						
		AF1	AF2	AF3	AF4	AF5	AF6	AF7
	UART	UART1 UART0 SDIO Clock IrDA UART2	I2C1 PWMG0 SDIO SPI0 Clock PWMG1	SWD Clock AoA/AoD AUX ADC LIN	DMIC TOUCH I2C1	AUX ADC Clock SPI0	LIN	XTALL
GPIO0[1]		UART1_TX	I2C1_SCL	SWCLK		ADC12	LIN_TXD	
GPIO1		UART1_RX	I2C1_SDA	SWDIO		ADC13	LIN_RXD	
GPIO8[1], [2]			PWMG0_PWM2		DMIC_CLK	ADC10		32K_XO
GPIO9			PWMG0_PWM3		DMIC_DAT			32K_XI
GPIO10[1]	DL_UART_RX	UART0_RX	SDIO_DATA2	CLK_AUXS_CIS				
GPIO11[1]	DL_UART_TX	UART0_TX	SDIO_DATA3					
GPIO12		UART0_RTS			TOUCH0	ADC14		
GPIO13		UART0_CTS			TOUCH1	ADC15		
GPIO14		SDIO_CLK	SPI0_SCK	BT_ANT0	I2C1_SCL			

GPIO	Flash Download	Alternate Functions						
		AF1	AF2	AF3	AF4	AF5	AF6	AF7
	UART	UART1 UART0 SDIO Clock IrDA UART2	I2C1 PWMG0 SDIO SPI0 Clock PWMG1	SWD Clock AoA/AoD AUX ADC LIN	DMIC TOUCH I2C1	AUX ADC Clock SPI0	LIN	XTALL
GPIO15		SDIO_CMD	SPI0_CSN	BT_ANT1	I2C1_SDA			
GPIO16		SDIO_DATA0	SPI0_MOSI	BT_ANT2				
GPIO17		SDIO_DATA1	SPI0_MISO	BT_ANT3				
GPIO18		SDIO_DATA2	PWMG0_PWM0					
GPIO19		SDIO_DATA3	PWMG0_PWM1					
GPIO24		LPO_CLK	PWMG0_PWM4	ADC2				
GPIO25		IRDA	PWMG0_PWM5	ADC1				
GPIO28			I2S_MCLK	ADC4	TOUCH2	CLK_AUXS_CIS		
GPIO32			PWMG1_PWM0		TOUCH6			
GPIO34			PWMG1_PWM2		TOUCH8	SPI0_CSN		
GPIO36			PWMG1_PWM4		TOUCH10	SPI0_MISO		
GPIO40		UART2_RX		LIN_RXD				
GPIO41		UART2_TX		LIN_TXD				
GPIO48								

	Flash Download	Alternate Functions						
		AF1	AF2	AF3	AF4	AF5	AF6	AF7
GPIO	UART	UART1 UART0 SDIO Clock IrDA UART2	I2C1 PWMG0 SDIO SPI0 Clock PWMG1	SWD Clock AoA/AoD AUX ADC LIN	DMIC TOUCH I2C1	AUX ADC Clock SPI0	LIN	XTALL

(1) Due to power-up glitches, the following GPIO pins are not recommended for applications sensitive to power-up fluctuations, such as LEDs or motor control: GPIO0, GPIO8, GPIO10, and GPIO11.

(2) It is not recommended to connect GPIO8 to externally touchable peripherals, such as buttons or touch sensors. If it must be connected, an ESD protection diode is required.

4. Functional Description

4.1 Wi-Fi/Bluetooth Transceiver

The BK7236 integrates a high-performance Wi-Fi/Bluetooth transceiver. The transceiver incorporates two on-chip baluns. On the receive side, the on-chip balun converts the single-ended (unbalanced) RF signal from the antenna into a differential (balanced) signal and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the on-chip balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with only one ANT pin connected to the antenna. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Clock Management

The primary clock sources available in the BK7236 are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator: it outputs clock signal XTALH
  - 26–360 MHz internal digitally controlled oscillator (DCO): it outputs clock signal CLK_DCO
  - Digital PLL (DPLL): it generates 320 MHz clock CLK_320M and 480 MHz clock CLK_480M
- Low-frequency clocks
  - 32 kHz (32.768 kHz) crystal oscillator: it outputs clock signal XTALL (BK7236QH4150 only)
  - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC
- Audio clock
  - Audio PLL (APLL): its default frequency is 98.304 MHz, and it outputs clock signal CLK_APLL

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz crystal oscillator XTALL (BK7236QH4150 only)
- 32 kHz clock signal derived from 26 MHz crystal oscillator
- 32 kHz internal oscillator ROSC

The BK7236 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- LPO_CLK: LPO_CLK clock

- I2S_MCLK: reference clock for external audio codec, derived from APLL
- CLK_AUXS_CIS: reference clock for external CMOS image sensor (CIS)

4.3 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

Power-on reset, brown-out reset, and AWDT watchdog reset reset the whole chip to its initial state. The DWDT watchdog reset's reset scope is configurable and can be configured to reset the whole chip.

Wake-up from shutdown mode triggers the whole system reset, while wake-up from deep sleep mode triggers the reset of digital blocks.

4.4 Power Management

4.4.1 Power Scheme

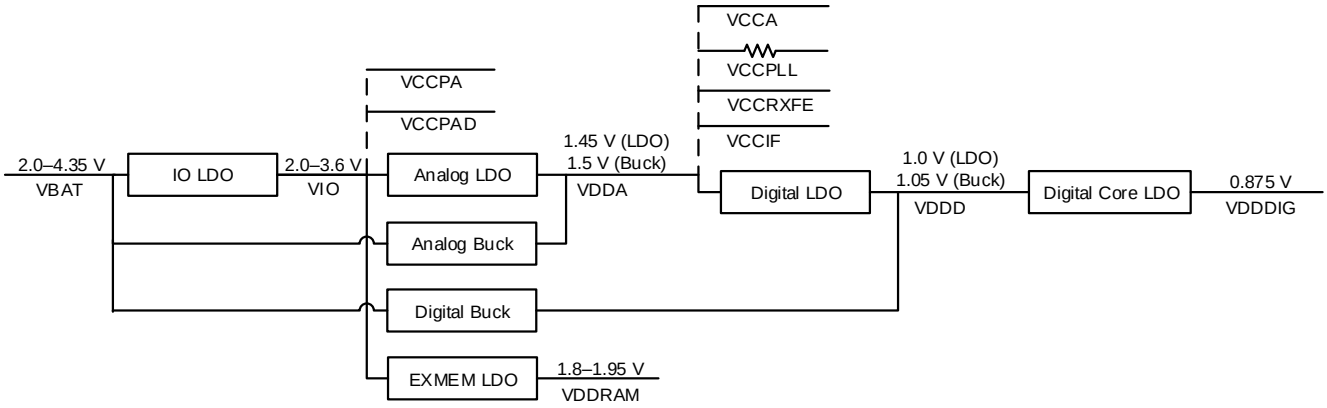
The power management system on the BK7236 includes two buck converters and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The VBAT is the external main chip supply ranging from 2.0 to 4.35 V. The VBAT generates VIO through the IO LDO regulator. In addition to being the power supply for Wi-Fi PA, the VIO is also the input supply of analog LDO, analog buck, digital buck, and EXMEM LDO. The VBAT also generates VDDA and VDDD through the analog buck converter and the digital buck converter, respectively. The LDOs and bucks generate the following main power supplies:

- VDDA: power supply for RF/analog blocks. It is externally connected to VCCA, VCCPLL, VCCRXFE, and VCCIF to supply power to Wi-Fi/Bluetooth transceiver, and internally provides power supply to XTAL directly.
- VDDDIG: power supply for digital domain. It provides power supply for the processor, memory, Wi-Fi and Bluetooth basebands, as well as various peripherals.
- VDDRAM: power supply for PSRAM.

Figure 4-1 shows the power distribution of the BK7236.

Figure 4-1 Internal Power Distribution



Note: Outputs from the buck converters and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-2 shows the power-up sequence of the BK7236.

Figure 4-2 BK7236 Power-up Sequence

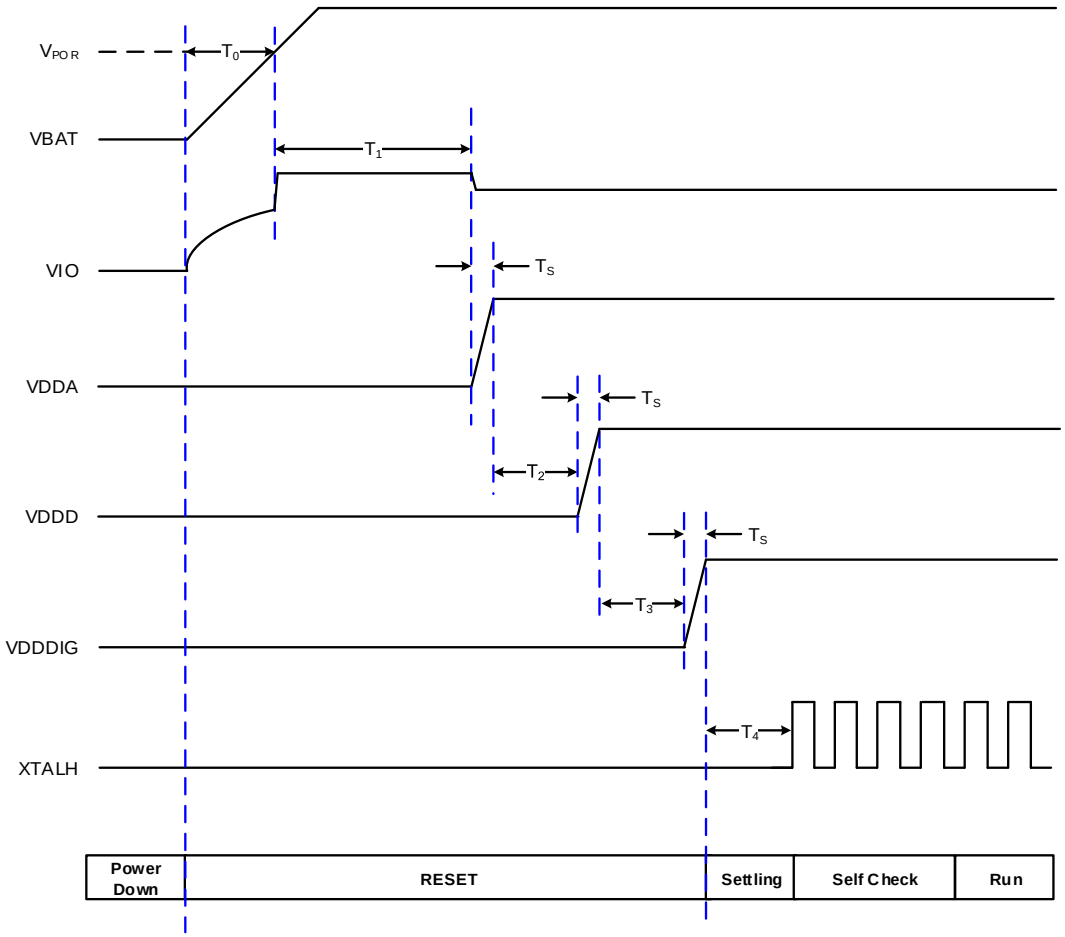


Table 4-1 Timing Parameters of Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{POR}	VBAT POR threshold	-	1.95	-	V
T_0	IO LDO settle time	200	-	-	μs
T_1(1)	IO LDO ready time	-	-	500	μs
T_2	Analog buck/LDO ready time	-	240	-	μs
T_3	Digital buck/LDO ready time	-	240	-	μs
T_4	Digital core LDO ready time/XTALH stable time	100	-	-	μs
T_S	LDO (excl. IO LDO) settle time	0	-	-	μs

(1) If the VBAT slew rate is greater than 3.3 kV/s, VIO will overshoot.

Figure 4-3 shows the power-down sequence of BK7236.

Figure 4-3 BK7236 Power-down Sequence

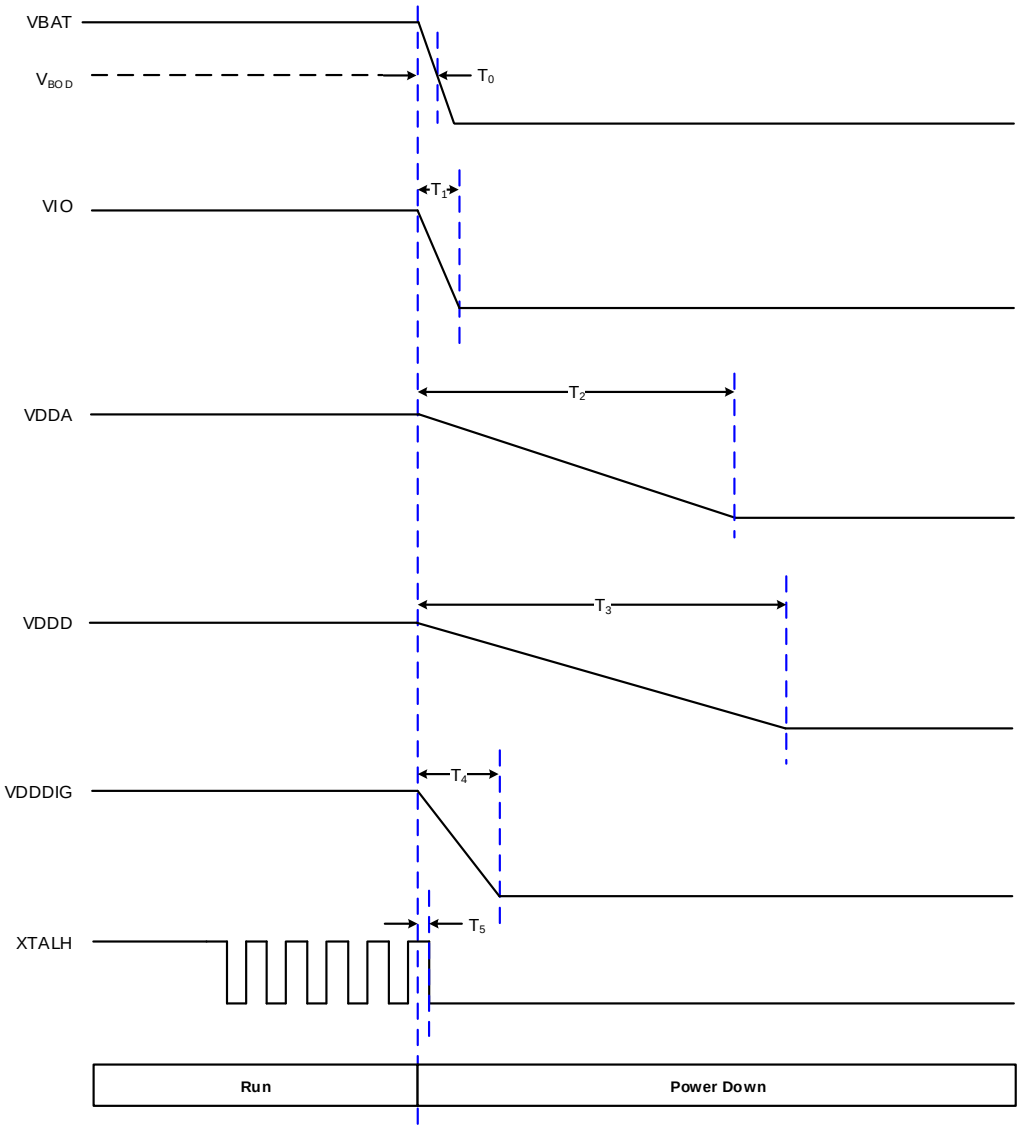


Table 4-2 Timing Parameters of Power-down Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{BOD}	VBAT BOD threshold	-	1.85	-	V
T_0	VBAT power-down time	-	400	-	μs
T_1	IO LDO power-down time	-	600	-	μs
T_2	Analog buck/LDO power-down time	-	400	-	ms

Parameter	Description	Min.	Typ.	Max.	Unit
T_3	Digital buck/LDO power-down time	-	500	-	ms
T_4	Digital core LDO power-down time	-	3.5	-	ms
T_5	XTALH power-down time	-	100	-	μs

4.4.2 Power Modes

The BK7236 supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the AON block. A GPIO event, an RTC event, or a touch sensor event can power up the system again. The retention register holds its content.

Sleep Mode: The MCU and all digital blocks stop their clocks. A GPIO event, an RTC event, a touch sensor event, a Wi-Fi MAC counter event, or a Bluetooth MAC counter event can bring the system back to active mode with normal voltage.

Active Mode: The MCU is active, and all peripherals are available.

4.5 General-purpose I/Os (GPIO)

The BK7236 has up to 23 GPIOs, which can be configured as either input or output. Most GPIOs are shared with alternate functions. Table 3-3 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.6 SPI Interface (SPI)

The BK7236 integrates an SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 40 MHz in both master and slave modes.

The SPI interface supports the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

4.7 UART Interfaces (UART)

The BK7236 includes three Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 6 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0) (BK7236QH4068/BK7236QH4050 only)
- Flash download (UART0)
- Programmable digital filter

4.8 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7236. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 80 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant
- SDIO card specification version 2.0 compliant

- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 40 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without CPU load

4.9 I2C Interface (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7236 embeds an I2C interface, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

4.10 USB Controller (USB)

The BK7236 embeds a USB high-speed (up to 480 Mbps) controller with an integrated transceiver. It can operate as a host or a device.

The USB controller features are the following:

- Compliant with the Universal Serial Bus Specification Rev 1.1 and 2.0
- Full-speed (FS) operation (up to 12 Mbps) and high-speed operation (up to 480 Mbps)
- One bidirectional control endpoint0
- Seven IN/OUT endpoints configurable to support bulk, interrupt or isochronous data transfer
- A FIFO of 8 Kbytes configurable to be allocated to 8 endpoints
- USB 2.0 Link Power Management (LPM) support

4.11 LIN Controller (LIN)

The Local Interconnect Network (LIN) controller is a communication controller that performs serial communication. It implements the data link layer of the LIN Protocol Specification. The LIN protocol uses a single master/multiple slave concept for the frame transfer between nodes of the LIN network.

The features of the LIN controller are listed here:

- Support of LIN specification 2.2A
- Backward compatibility to LIN 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 kbit/s and 20 kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface

4.12 GDMA Controllers (GDMA)

The BK7236 has two general-purpose DMA controllers (GDMA) with 8 DMA channels each to unload CPU activity. The 8 channels are shared by peripherals that have DMA capabilities.

The GDMA controllers can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controllers allow peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The GDMA controllers support channel isolation. The DMA channels can be configured as secure/non-secure and as privileged/unprivileged channels:

- A non-secure channel performs non-secure DMA transfers
- A secure channel can perform secure or non-secure DMA transfers, with
  - Secure or non-secure data read from the source address
  - Secure or non-secure data write to the destination address
  - Via a TrustZone-aware DMA AHB master port
- An unprivileged channel performs unprivileged DMA transfers
- A privileged channel performs privileged DMA transfers

A selection of peripherals on the BK7236 have DMA capabilities, including UART0, UART1, UART2, SPI0, SDIO, and AUX ADC.

4.13 PWM Groups (PWMG)

The BK7236 has two advanced-control PWM groups (PWMG). Each PWMG consists of up to four independent 32-bit auto-reload counters driven by four programmable prescalers. The PWMGs can generate pulse width

modulated signals for a variety of purposes, including input capture, pulse edge counting, or generation of output waveforms (output compare).

The features of one PWMG are listed here:

- Maximum four 32-bit up, down, or up-and-down auto-reload counters
  - PWM0 has a counter.
  - PWM1 has a counter (up-counting mode only).
  - PWM2 and PWM3 share a counter.
  - PWM4 and PWM5 share a counter.
- Maximum four 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- Maximum four Independent channels, among which:
  - PWM0/2/4
    - Input capture
    - Pulse edge counting
    - PWM generation (edge or center-aligned mode)
  - PWM1
    - Independent simple waveform generation (up-counting mode)
    - Coupled waveform (reverse or identical) generation when coupled with PWM0
- Two channels PWM3/5 capable of generating coupled waveforms (reverse or identical) when coupled with PWM2/4 respectively
- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

Table 4-3 below provides the description of PWM signals.

Table 4-3 PWM Signals

GPIO	PWM Pin Name	Signal Type	Description
PWMG0			
GPIO18	PWMG0_PWM0	I/O	PWM0 channel of PWMG0
GPIO19	PWMG0_PWM1	I/O	PWM1 channel of PWMG0 PWM1 can work independently to generate simple waveforms or couple with PWM0 (with deadtime insertion) to generate reverse or identical waveforms of PWM0.
GPIO8	PWMG0_PWM2	I/O	Available on BK7236QH4150 PWM2(1) channel of PWMG0
GPIO9	PWMG0_PWM3	I/O	Available on BK7236QH4150 PWM3(1) channel of PWMG0 PWM3 can couple with PWM2 (with deadtime insertion) to generate reverse or identical waveforms of PWM2.
GPIO24	PWMG0_PWM4	I/O	PWM4(2) channel of PWMG0
GPIO25	PWMG0_PWM5	I/O	Available on BK7236QH4068/BK7236QH4050 PWM5(2) channel of PWMG0 PWM5 can couple with PWM4 (with deadtime insertion) to generate reverse or identical waveforms of PWM4.
PWMG1			
GPIO32	PWMG1_PWM0	I/O	PWM0 channel of PWMG1
GPIO34	PWMG1_PWM2	I/O	PWM2 channel of PWMG1
GPIO36	PWMG1_PWM4	I/O	PWM4 channel of PWMG1

(1) When PWM2 and PWM3 are enabled simultaneously, they cannot generate waveforms with different duty cycles.

(2) When PWM4 and PWM5 are enabled simultaneously, they cannot generate waveforms with different duty cycles.

4.14 Digital Microphone Interface (DMIC)

The BK7236 has a digital microphone interface that supports two digital microphones. The PDM performs 8:1 CIC decimation, and the PCM sampling rate can be up to 384 kHz when the PDM clock frequency is 3.072 MHz.

4.15 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 12-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rate from 12.5 kHz to 812.5 kHz
- 12-bit resolution
- Up to 8 external analog input channels: ADC1/2/4/10/12/13/14/15
- Five internal dedicated channels:
  - VBAT monitoring channel (VBAT/2, VBAT/3, VBAT/5, or VBAT/7), connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - TSSIO, connected to ADC8
  - Touch OUT_TD, connected to ADC9
  - Internal debug channel, connected to ADC11
- Conversion modes:
  - One-shot mode
  - Software control mode
  - Continuous mode

4.16 Timer Groups (TIMG)

The BK7236 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, division factor between 1 and 16
- Capable of reading the real-time value of the counter

4.17 Watchdog Timers (WDT)

The BK7236 has two watchdog timers, the digital power domain watchdog timer (DWDT) and the AON power domain watchdog timer (AWDT). The purpose of the watchdog timers is to detect and recover from failures or malfunctions. The watchdog timers trigger a reset on expiry of a specified time period.

The DWDT runs on the 32 kHz LPO_CLK clock (division factor 2/4/8/16) and has a maximum programmable period of up to 32.768 (2^16/2 kHz) seconds. The AWDT runs on the ROSC and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

4.18 Real-time Counter (RTC)

The real-time counter (RTC) module features a 64-bit counter and a tick event generator. The RTC runs on the 32 kHz LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

4.19 IrDA Interface (IrDA)

The BK7236 embeds a hardware IrDA interface that supports waveform analysis and waveform generation. It monitors the start of infrared signals, records the sequence of infrared waveforms, stores the waveforms in the RX FIFO for software analysis, and writes the waveforms to be sent to the TX FIFO when sending, thereby enabling the analysis and transmission of any infrared protocol.

The IrDA has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

4.20 Temperature Sensor

The BK7236 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read from the AUX ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

4.21 Touch Sensor (TOUCH)

The BK7236 has up to six capacitive sensing I/Os, which immediately detect capacitance changes induced by touch or proximity of objects.

4.22 Security

The BK7236 provides state-of-the-art security based on a powerful security architecture. It integrates a total security solution for Internet of Things (IoT), IoT Platform Security Suite (IPSS). The IPSS aims to set up a top-secret execution environment for IoT devices. With the state-of-the-art security technology, it is intended for power/cost/resource sensitive IoT market applications.

The IPSS introduces a fundamental software IP solution for cryptograph and system security control. The key features of the IPSS include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine

System Architecture

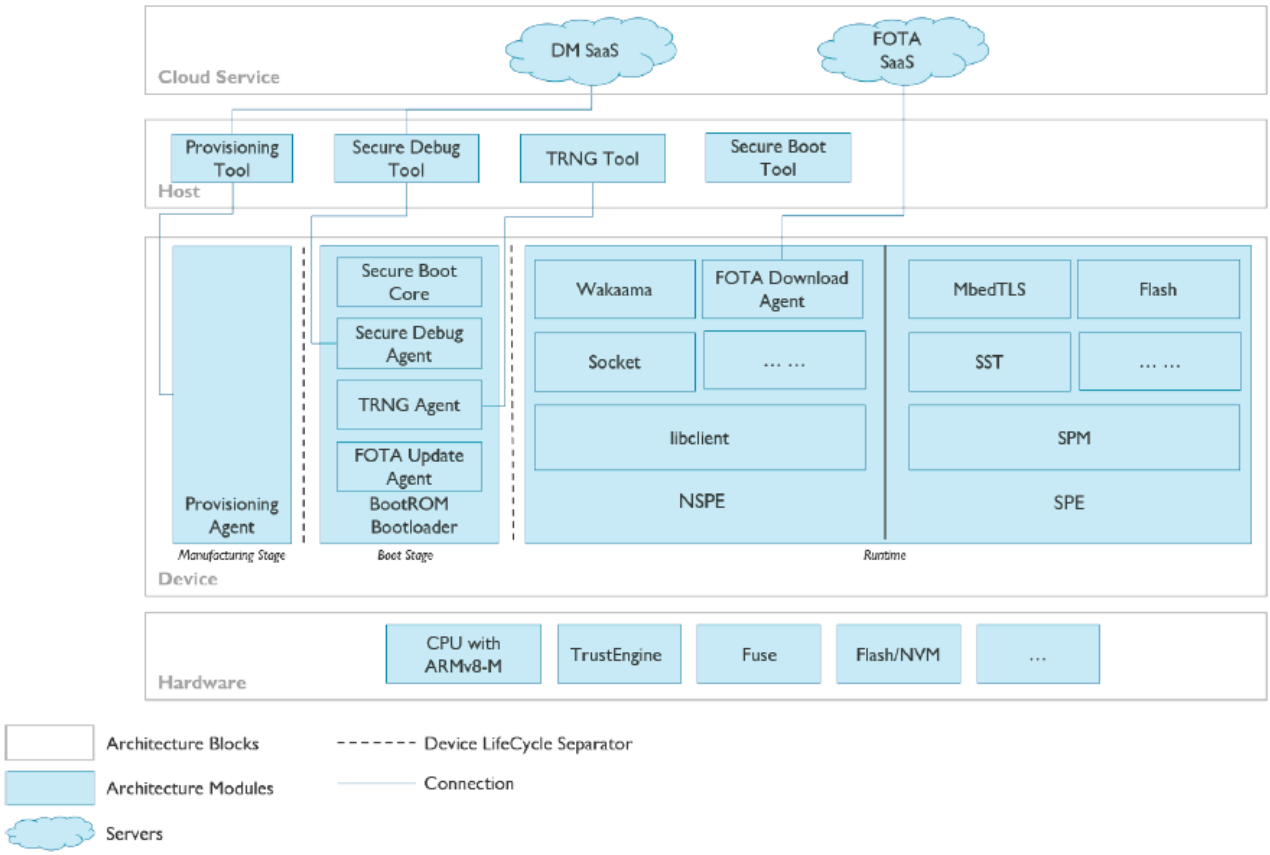
The IPSS software implements an all-round device-to-cloud security architecture, including:

- Provisioning mechanism in the manufacturing stage.
- Secure boot, secure debug, TRNG calibration, and FOTA update in the device boot stage.
- Secure connection and FOTA download in the device run-time stage.

IPSS also introduces a remote management solution to enable users to access, monitor and manage IoT devices in a secure manner. The remote management solution includes FOTA SaaS, Secure Debug SaaS, and Provisioning SaaS.

The following figure shows the architecture of the IPSS system.

Figure 4-4 Security Architecture of the IPSS System



4.22.1 Secure Boot

The secure boot solution provides the legitimacy and trustworthiness for images running on devices. It ensures that only official images which are published from OEMs are executable.

The secure boot functions include following aspects:

- Image verification
- Image encryption
- Extended program execution
- Image anti-rollback protection

4.22.2 Secure Debug

Secure debug provides a reliable mechanism for enabling the debug feature of a device after the device deployment.

Debug is one of the most commonly-used features in the device. With the debug feature, you can access all the device data, including the device firmware and the device root key.

4.22.3 FOTA

The FOTA solution implements a series of light-weight and trustworthy firmware upgrade interaction between IoT devices and servers, which includes downloading, verification, and installation.

4.22.4 Provisioning

Provisioning is the process to initialize secure credentials onto devices. It is required to happen in a secure environment such as the product line in the manufacturing stage.

The provisioning solution provides a full secure mechanism from the cloud server to devices. It keeps the security and integrity of provisioning materials, such as the device ID, model key, and the secure boot/secure debug public key hash, also keeps the device top secret such as the device root key that occurs only on the device side.

4.22.5 Secure Connection

The secure connection feature uses Mbed TLS to provide connection security in the transport layer over UDP. The key exchange method is Pre-Shared Key (PSK). The PSK's deployment happens in the manufacturing stage.

Mbed TLS provides cryptograph and SSL/TLS capabilities with TLS 1.1 and TLS 1.2.

4.22.6 BootROM

IPSS includes the BootROM reference code which is integrated with the secure boot solution.

There are primary boot and recovery boot paths in the BootROM.

- Primary boot is the main boot path. Normally devices should boot to the primary path.
- Recovery boot is the secondary boot path.

4.22.7 Bootloader

IPSS includes the Bootloader reference code which is integrated with the secure debug, provisioning, TRNG calibration, and FOTA solution.

In the primary bootloader, the secure debug agent, provisioning agent, and TRNG agent are integrated. The primary bootloader boots to the next image—TEE_M.

In the recovery bootloader, both the secure debug agent, TRNG agent, and the FOTA update agent are integrated. The recovery bootloader does not boot to any images.

4.22.8 TEE_M

IPSS introduces TEE_M. TEE_M provides an implementation of secure world software for Armv8-M, which follows Arm Platform Security Architecture (PSA) PSA_Firmware_Framework_1.0-bet0. IPSS TEE_M provides the following services by default:

- Secure Storage: The Secure Storage (Only supports Protected Storage) service supports PSA_Storage_API-1.0-bet2 without extended functions.
- Crypto: The Crypto service supports PSA_Cryptography_API_Reference_1.0_bet1.
- DTLS: DTLS (leverages Mbed TLS) is integrated in TEE_M.

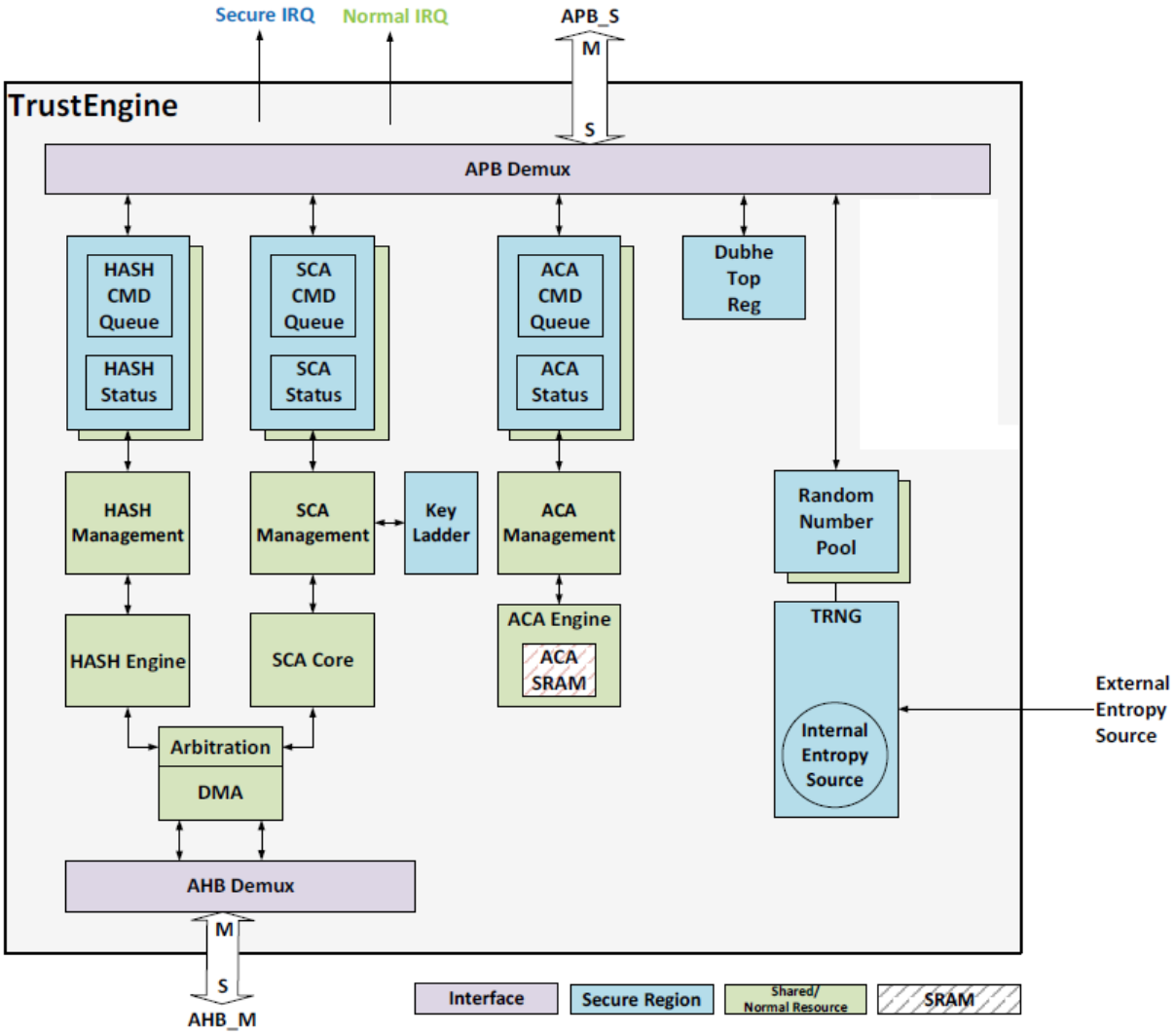
4.22.9 TrustEngine

IPSS introduces TrustEngine as a secure component in the system. It provides the following features:

- High security assurance. The crypto engine supports key ladders, lifecycle management and True Random Number Generator (TRNG) which enhance the system security.
- High performance and low power for encryption/decryption operation. This is achieved by TrustEngine internal cryptography engines.
- Reduction of software complicity in security. Some security functions are implemented in TrustEngine hardware, which can reduce the risk of sensitive information leakage to non-secure hosts.

The following figure shows the TrustEngine top-level architecture.

Figure 4-5 TrustEngine Top-Level Architecture



4.22.9.1 Features

TrustEngine includes the following features:

- Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
- Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
- Digest schemes, SHA1/224/256
- Digest scheme, SM3
- Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
- Asymmetric scheme, SM2

- Key ladder for key management
- Lifecycle management
- True random number generator

4.22.9.2 Supported Standards and Specifications

TrustEngine is compliant with the following standards:

- FIPS PUB 180-4: Secure Hash Standard (SHS)
- FIPS PUB 197: Advanced Encryption Standard (AES)
- NIST SP 800-38A Recommendation for Block Cipher Modes of Operation-Methods and Techniques
- NIST SP 800-38B Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication
- NIST SP 800-38C Recommendation for Block Cipher Modes of Operation-the CCM Mode for Authentication and Confidentiality
- NIST SP 800-38D, Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC
- NIST SP 800-90B Recommendation for the Entropy Sources Used for Random Bit Generation
- SM2 Public Key Cryptographic Algorithm Based on Elliptic Curves (GB/T 32918-2016)
- SM3 Cryptographic Hash Algorithm (GB/T 32905-2016)
- SM4 Block Cipher Algorithm (GB/T 32907-2016)

4.22.9.3 Components

TrustEngine consists of five major function blocks.

- Symmetric Cryptography Accelerator (SCA)
- Asymmetric Cryptography Accelerator (ACA)
- HASH engine
- One-time programmable storage access controller
- True random number generator

Symmetric Cryptography Accelerator (SCA)

SCA in TrustEngine is responsible for data encryption/decryption using the symmetric cryptography algorithm. The data encryption/decryption operations are performed through the SCA engine by sending special commands to TrustEngine.

Asymmetric Cryptography Accelerator (ACA)

The ACA engine in TrustEngine is responsible for accelerating the asymmetric cryptography, such as:

- Asymmetric encryption and decryption: RSA and ECC
- Digital signature and verification: RSA signatures and ECDSA
- Key exchange: DH (Diffie-Hellman) and ECDH

HASH Accelerator

The HASH engine in TrustEngine is responsible for digest calculation. The digest of certain data can be calculated through the HASH engine by sending special commands to TrustEngine.

True Random Number Generator

The True Random Number Generator (TRNG) generates the random bits using the internal entropy source (ring oscillator inverter chain) or the external entropy source. The random bits are required by both secure and non-secure hosts.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Chip power supply voltage	-0.3	4.5	V
VIO	IO LDO output voltage	-0.3	4.0	V
VCCPA	Supply voltage for PA	-0.3	4.0	V
VCCPAD	Supply voltage for PA driver	-0.3	4.0	V
VCCIF	Supply voltage for IF	-0.3	1.8	V
VCCRXFE	Supply voltage for RX	-0.3	1.8	V
VCCPLL	Supply voltage for RF PLL	-0.3	1.8	V
VCCA	Supply voltage for analog	-0.3	1.8	V
VDDA	Analog LDO output voltage	-0.3	1.8	V
	Analog buck output voltage	-0.3	1.8	V
VDDD	Digital LDO output voltage	-0.3	1.2	V
	Digital buck output voltage	-0.3	1.2	V
VDDDIG	Digital core LDO output voltage	-0.3	1.1	V
VDDRAM	EXMEM LDO output voltage	-0.3	2.1	V
SWA	Analog buck switch output voltage	-0.3	4.5	V
SWD	Digital buck switch output voltage	-0.3	4.5	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	°C

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001	-	±2000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002	-	±500	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.(1)	Typ.	Max.	Unit
VBAT(2)	Chip power supply voltage	2.0	3.3	4.35	V
VBAT slew rate	-	300	-	-	mV/ms
VIO	IO LDO output voltage	2.0	-	3.6	V
VCCPA(2)	Supply voltage for PA	2.0	-	3.6	V
VCCPAD(2)	Supply voltage for PA driver	2.0	-	3.6	V
VCCIF	Supply voltage for IF	-	1.45	-	V
VCCRXFE	Supply voltage for RX	-	1.45	-	V
VCCPLL	Supply voltage for RF PLL	-	1.45	-	V
VCCA	Supply voltage for analog	-	1.45	-	V
VDDA	Analog LDO output voltage	-	1.45	-	V
	Analog buck output voltage	-	1.5	-	V
VDDD	Digital LDO output voltage	-	1.0	-	V
	Digital buck output voltage	-	1.05	-	V
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
T_{OPR}	Operating temperature range	-40	-	105	°C

(1) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. Care must be taken when operating at the minimum specified voltage.

(2) To ensure WLAN performance, the ripple on the supply must be less than Vpp = 100 mV.

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VIO	-	VIO + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VIO	V
VOH	High-level output voltage	-	0.8 VIO	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VIO	V
I_{DRV}	I/O output drive strength	-	5	-	20	mA
R_{PU}	Weak pull-up resistor	-	-	40	-	kΩ
R_{PD}	Weak pull-down resistor	-	-	44	-	kΩ

5.5 IO LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO output voltage	2.0	3.3	3.6	V
Load current	-	-	-	500	mA

5.6 Analog LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog LDO output voltage	-	1.45	-	V
Load current	-	-	-	150	mA

5.7 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital LDO output voltage	-	1.0	-	V
Load current	-	-	-	100	mA

5.8 Core LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
Load current	-	-	-	100	mA

5.9 EXMEM LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
Load current	-	-	-	50	mA

5.10 Analog Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog buck output voltage	-	1.5	-	V
Load current	-	-	-	150	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	mΩ
Inductor saturation current	-	200	-	-	mA

5.11 Digital Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital buck output voltage	-	1.05	-	V
Load current	-	-	-	100	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz

Parameter	Description	Min.	Typ.	Max.	Unit
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	mΩ
Inductor saturation current	-	200	-	-	mA

5.12 26 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	26	-	MHz
ΔF/F0	Frequency tolerance	25 °C	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 °C crystal	-20	-	+20	ppm
		-30 to 85 °C crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7.3	12	pF
TS	Trim sensitivity	-40 to 105 °C crystal	-	32	-	ppm/pF
		-30 to 85 °C crystal	-	17	-	ppm/pF

5.13 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11b: 11 Mbps DSSS	-	17.5	-	mA
	11g: 54 Mbps OFDM	-	17.5	-	mA
	11n: MCS7, HT20	-	17.5	-	mA
	11n: MCS7, HT40	-	18.5	-	mA
	11ax: MCS7, HE20	-	17.5	-	mA
TX current	11b: 11 Mbps DSSS @ 19 dBm	-	235	-	mA

Parameter	Condition	Min.	Typ.	Max.	Unit
	11g: 54 Mbps OFDM @ 17 dBm	-	200	-	mA
	11n: MCS7, HT20 @ 16 dBm	-	189	-	mA
	11n: MCS7, HT40 @15 dBm	-	182	-	mA
	11ax: MCS7, HE20 @ 16 dBm	-	188	-	mA
Sleep Mode					
Sleep	-	-	43	-	μA
Deep sleep	-	-	16	-	μA
Shutdown Mode					
Shutdown	-	-	2.5	-	μA

5.14 WLAN RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	-	-98	-	dBm
	2 Mbps DSSS	-	-94.5	-	dBm
	5.5 Mbps DSSS	-	-92	-	dBm
	11 Mbps DSSS	-	-89	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77.5	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	54 Mbps OFDM	-	-76.5	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HT20, MCS0	-	-92	-	dBm
	HT20, MCS1	-	-91	-	dBm
	HT20, MCS2	-	-88	-	dBm
	HT20, MCS3	-	-86	-	dBm
	HT20, MCS4	-	-82	-	dBm
	HT20, MCS5	-	-78	-	dBm
	HT20, MCS6	-	-76.5	-	dBm
	HT20, MCS7	-	-75	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz (10% PER for 4096 octet PSDU, LDPC)	HT40, MCS0	-	-87.5	-	dBm
	HT40, MCS1	-	-87	-	dBm
	HT40, MCS2	-	-85	-	dBm
	HT40, MCS3	-	-82.5	-	dBm
	HT40, MCS4	-	-79	-	dBm
	HT40, MCS5	-	-75	-	dBm
	HT40, MCS6	-	-74	-	dBm
	HT40, MCS7	-	-71.5	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HE20, MCS0	-	-92	-	dBm
	HE20, MCS1	-	-90.5	-	dBm
	HE20, MCS2	-	-87.5	-	dBm
	HE20, MCS3	-	-85	-	dBm
	HE20, MCS4	-	-81	-	dBm
	HE20, MCS5	-	-77.5	-	dBm
	HE20, MCS6	-	-75.5	-	dBm
	HE20, MCS7	-	-74	-	dBm
Sensitivity - IEEE 802.11ax, 40 MHz (10% PER for 4096 octet PSDU, LDPC)	HE40, MCS0	-	-88.5	-	dBm
	HE40, MCS1	-	-87.5	-	dBm
	HE40, MCS2	-	-85.5	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
	HE40, MCS3		-	-82	-	dBm
	HE40, MCS4		-	-77	-	dBm
	HE40, MCS5		-	-75	-	dBm
	HE40, MCS6		-	-74	-	dBm
	HE40, MCS7		-	-72	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11g: 6–54 Mbps (10% PER, 1000 octets)		-	0	-	dBm
	11n: MCS0–7 (10% PER, 4096 octets)		-	0	-	dBm
	11ax: MCS0–7 (10% PER, 4096 octets)		-	0	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	50	-	dB
	2 Mbps DSSS	-74 dBm	-	45	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	43	-	dB
	11 Mbps DSSS	-70 dBm	-	40	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g (10% PER for 1000 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	43	-	dB
	54 Mbps OFDM	-62 dBm	-	27	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n	HT20, MCS0	-79 dBm	-	43	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
(10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT20, MCS7	-61 dBm	-	21	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT40, MCS0	-76 dBm	-	34	-	dB
	HT40, MCS7	-58 dBm	-	25	-	dB
Adjacent channel (±20 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE20, MCS0	-79 dBm	-	43	-	dB
	HE20, MCS7	-61 dBm	-	26	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE40, MCS0	-76 dBm	-	32	-	dB
	HE40, MCS7	-58 dBm	-	27	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-60	-	dBm
	> 1 GHz		-	-50	-	dBm

5.15 WLAN RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX Power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	21	-	dBm
	11 Mbps DSSS	-	21	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	18	-	dBm
	54 Mbps OFDM	-	18	-	dBm
TX power - IEEE 802.11n	HT20, MCS0	-	17	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
(EVM compliant)	HT20, MCS7	-	17	-	dBm
	HT40, MCS0	-	17	-	dBm
	HT40, MCS7	-	16	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	17	-	dBm
	HE20, MCS7	-	17	-	dBm
	HE40, MCS0	-	17	-	dBm
	HE40, MCS7	-	16	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-50	-	dBm
	> 1 GHz	-	-45	-	dBm

5.16 Bluetooth LE RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-97	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 1 MHz adjacent channel	-	-	0	-	dB
C/I -1 MHz adjacent channel	-	-	0	-	dB
C/I 2 MHz adjacent channel	-	-	-26	-	dB
C/I -2 MHz adjacent channel	-	-	-27	-	dB
C/I 3 MHz adjacent channel	-	-	-28	-	dB
C/I -3 MHz adjacent channel	-	-	-29	-	dB
C/I > 3 MHz adjacent channel	-	-	-50	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I < -3 MHz adjacent channel	-	-	-50	-	dB
Out-of-band blocking	30–2000 MHz	-10	-	-	dBm
	2003–2399 MHz	-12	-	-	dBm
	2484–2997 MHz	-12	-	-	dBm
	3000 MHz–12.75 GHz	-2	-	-	dBm
Intermodulation	-	-	-32	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-94	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	7	-	dB
C/I 2 MHz adjacent channel	-	-	0	-	dB
C/I -2 MHz adjacent channel	-	-	3	-	dB
C/I 4 MHz adjacent channel	-	-	-26	-	dB
C/I -4 MHz adjacent channel	-	-	-30	-	dB
C/I 6 MHz adjacent channel	-	-	-30	-	dB
C/I -6 MHz adjacent channel	-	-	-39	-	dB
C/I > 6 MHz adjacent channel	-	-	-22	-	dB
C/I < -6 MHz adjacent channel	-	-	-22	-	dB
Out-of-band blocking	30–2000 MHz	-	-30	-	dBm
	2003–2399 MHz	-	-35	-	dBm
	2484–2997 MHz	-	-35	-	dBm
	3000 MHz–12.75 GHz	-	-17	-	dBm
Intermodulation	-	-	-32	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	-102	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	3	-	dB
C/I 1 MHz adjacent channel	-	-	-15	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I -1 MHz adjacent channel	-	-	-16	-	dB
C/I 2 MHz adjacent channel	-	-	-34	-	dB
C/I -2 MHz adjacent channel	-	-	-40	-	dB
C/I 3 MHz adjacent channel	-	-	-42	-	dB
C/I -3 MHz adjacent channel	-	-	-43	-	dB
C/I > 3 MHz adjacent channel	-	-	-41	-	dB
C/I < -3 MHz adjacent channel	-	-	-42	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	-99	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	5	-	dB
C/I 1 MHz adjacent channel	-	-	-2	-	dB
C/I -1 MHz adjacent channel	-	-	-3	-	dB
C/I 2 MHz adjacent channel	-	-	-30	-	dB
C/I -2 MHz adjacent channel	-	-	-31	-	dB
C/I 3 MHz adjacent channel	-	-	-31	-	dB
C/I -3 MHz adjacent channel	-	-	-40	-	dB
C/I > 3 MHz adjacent channel	-	-	-36	-	dB
C/I < -3 MHz adjacent channel	-	-	-36	-	dB

5.17 Bluetooth LE RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
TX power	-	-20	6	15	dBm

Parameter		Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf1avg	-	225	245	275	kHz
	Δf2max	-	185	235	-	kHz
	Δf2avg/Δf1avg	-	0.8	0.93	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	2	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	-50	-	dBm
	±5 MHz offset	-	-	-51	-	dBm
	>±5 MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf1avg	-	-	488	-	kHz
	Δf2max	-	-	469	-	kHz
	Δf2avg/Δf1avg	-	-	0.93	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	1.5	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 125 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm
Modulation	Δf1avg	-	225	245	275	kHz

Parameter		Condition	Min.	Typ.	Max.	Unit
characteristics	Δf1max	-	185	246	-	kHz
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	1.5	150	kHz
	Max $\|f_0 - f_n\|$ n = 1, 2, 3…k	-	-	1.5	50	kHz
	$\|f_0 - f_3\|$	-	-	1.5	19.2	kHz
	$\|f_n - f_{n-3}\|$ n = 7, 8, 9…k	-	-	1.5	19.2	kHz/48 μs
Bluetooth LE 500 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm

5.18 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	0.2	-	13	MHz
Conversion time	-	-	16	-	Cycle
V_{REF}	Internal	-	1.1	-	V
	External	-	VIO/3	-	V
Input voltage range	-	0	-	V_{REF}*N(1)	V
Input impedance	-	10	-	-	MΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-1	-	3	LSB
INL	-	-5	-	5	LSB
ENOB	-	-	10	-	Bit
SNDR	-	-	62	-	dB
SFDR	-	-	77	-	dB
$T_{STARTUP}$	-	-	5	-	μs
Current consumption	-	-	200	-	μA

(1) N is the input voltage division factor. N=1, 2, 3, or 4.

6. Package Information

6.1 QFN40 5 x 5 x 0.75 mm Package

BK7236QH4050 and BK7236QH4150 come in a QFN40 5 x 5 x 0.75 mm package.

Figure 6-1 QFN40 5 x 5 x 0.75 mm Package Outline

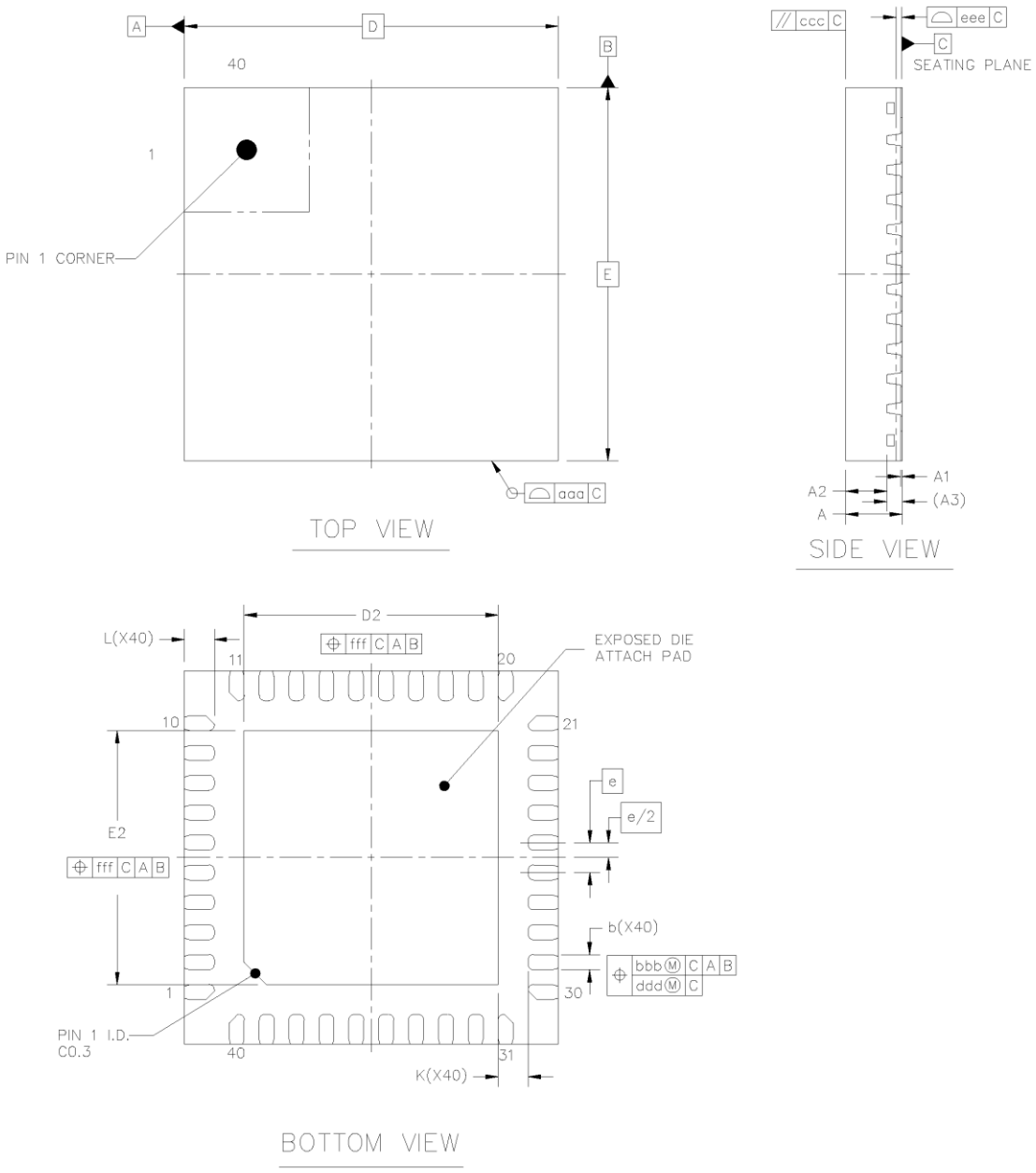


Table 6-1 QFN40 5 x 5 x 0.75 mm Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
L	0.30	0.40	0.50
K	0.40 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

6.2 QFN40 5 x 5 x 0.9 mm Package

BK7236QH4068 comes in a QFN40 5 x 5 x 0.9 mm package.

Figure 6-2 QFN40 5 x 5 x 0.9 mm Package Outline

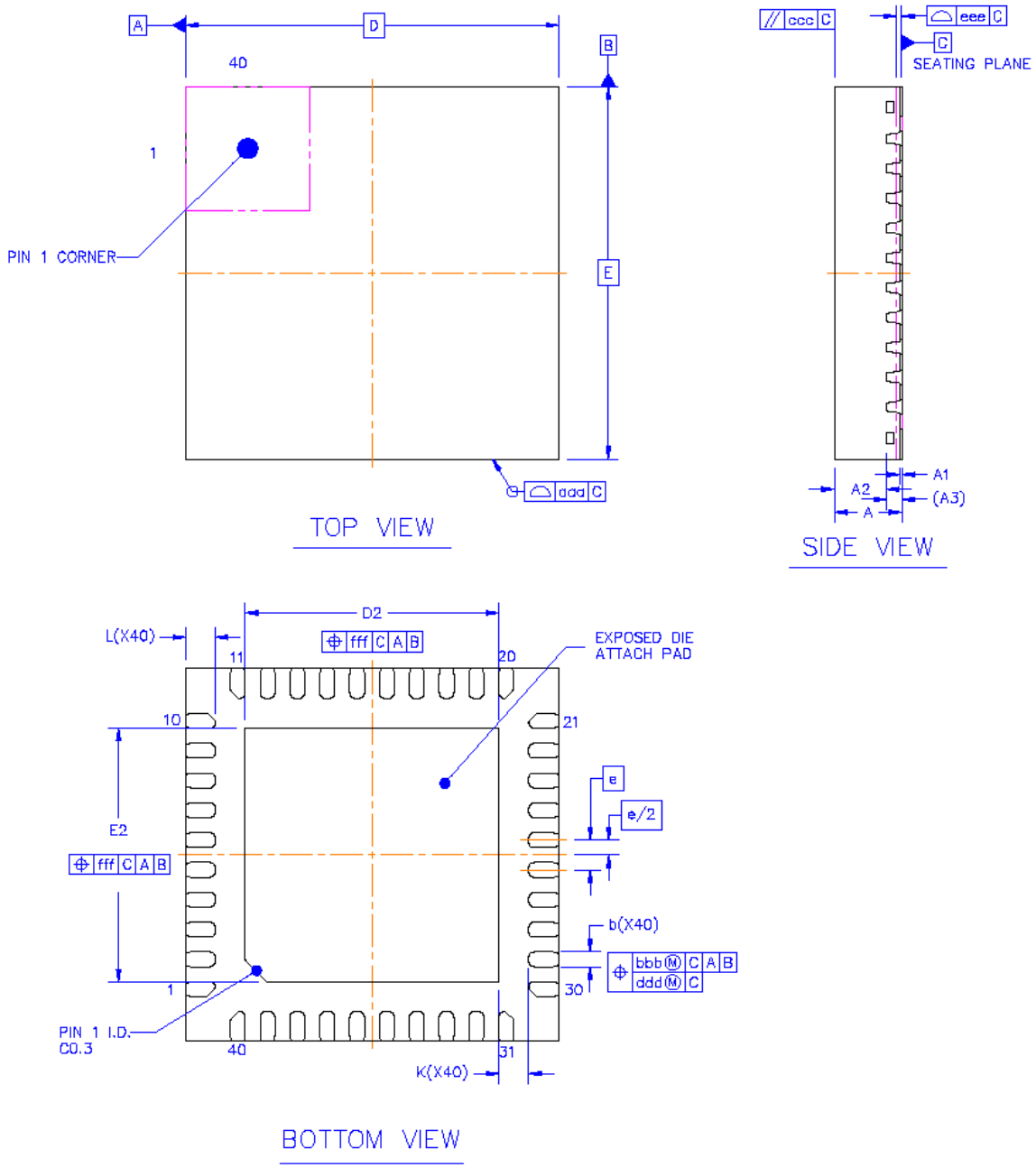
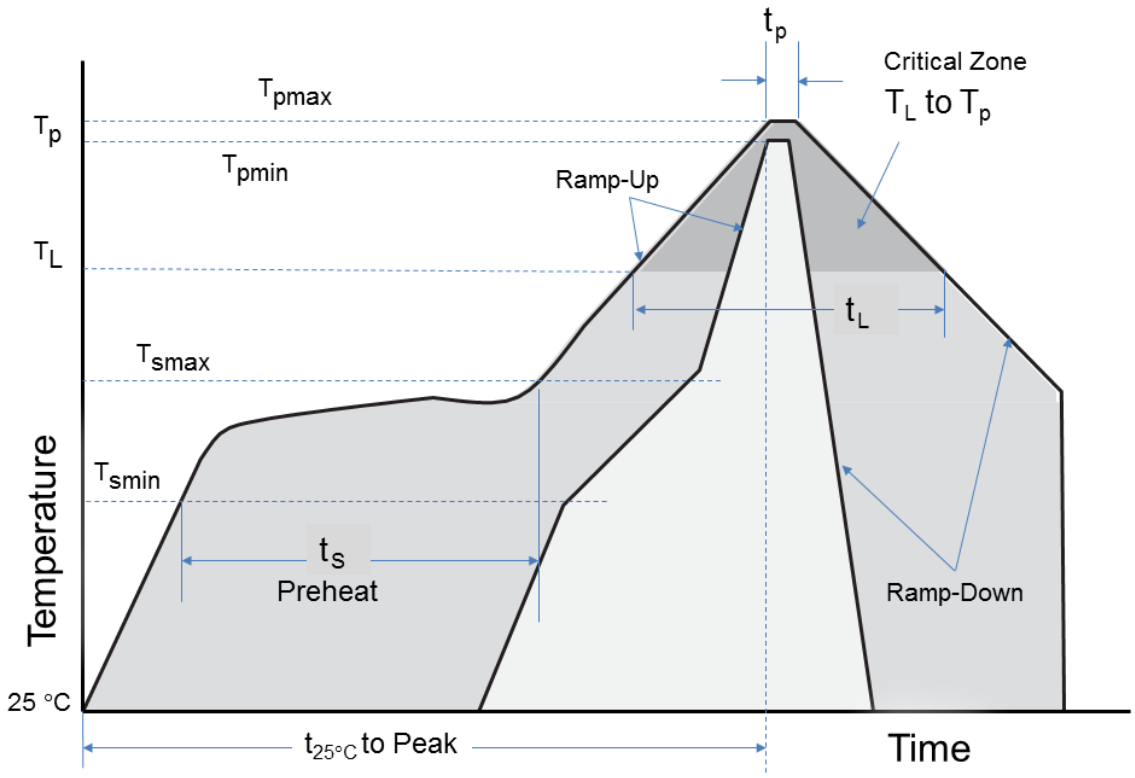


Table 6-2 QFN40 5 x 5 x 0.9 mm Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
A2	-	0.70	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
L	0.30	0.40	0.50
K	0.40 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 °C/s max.
Preheat	Temperature min. (T_{smin})	150 °C
	Temperature max. (T_{smax})	200 °C
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 °C
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 °C
Time within 5 °C of actual peak temperature (t_p)		20 s to 40 s

Profile Feature	Specification
Ramp-down rate	6 °C/s max.
Time 25 °C to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Ordering Code Scheme

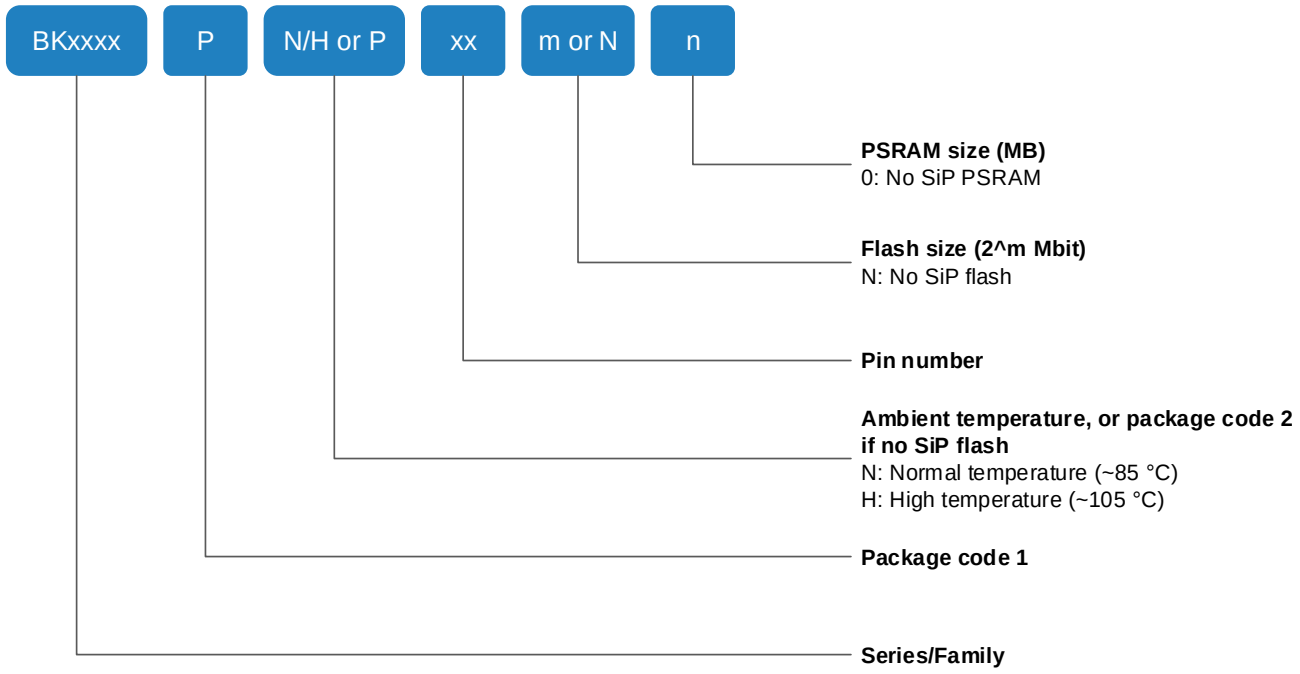


Table 8-1 Ordering Information

Ordering Code	Package	SiP(1) Flash	SiP PSRAM	Packing	Minimum Ordering Qty (MOQ)(2)
BK7236QH4068	5 mm x 5 mm x 0.9 mm QFN40	8 MB	8 MB	Tape and Reel	3000
BK7236QH4050	5 mm x 5 mm x 0.75 mm QFN40	4 MB	-	Tape and Reel	3000
BK7236QH4150(3)	5 mm x 5 mm x 0.75 mm QFN40	4 MB	-	Tape and Reel	3000

(1) A system in a package (SiP) refers to flash/PSRAM enclosed in the package.

(2) The MOQ for customized or exclusive ordering codes is one wafer lot. Please consult your sales representative for the exact quantity.

(3) The BK7236QH4150 deviates from the standard naming convention to distinguish it from the BK7236QH4050, which has the same memory and package configuration but different pin assignments.

Revision History

Version	Date	Description
0.1	2022/7/8	Initial release
1.0	2022/12/14	Updated the pin assignments for pin # 39 and pin # 40 in Section 3 Pin Descriptions
1.1	2023/3/2	• General wording fixes • Updated TX power in Section 1 Features • Updated compliance with Bluetooth Specification to Bluetooth 5.4 in Section 1 Features and Section 2 Overview • Updated core frequency in subsection Core of Section 1 Features • Removed JTAG from, added SPI flash download and SWD interface to subsection Core of Section 1 Features • Removed cache from subsection Memory of Section 1 Features • Updated full-speed USB to high-speed USB in Section 1 Features • Updated the number of GDMA controllers and GDMA channel number in Section 1 Features and Section 4.12 GDMA Controllers (GDMA) • Updated the number of PWM in Section 1 Features • Updated the resolution of SAR ADC in Section 1 Features and Section 4.15 Auxiliary ADC (AUX ADC) • Updated Figure 2-1 BK7236 Block Diagram in Section 2 Overview • Updated pin assignments of the QFN40 package and GPIO mapping of PWM in Section 3 Pin Descriptions • Corrected the description of clock signals can be output by GPIOs in Section 4.2 Clock Management • Updated SPI frequency in Section 4.6 SPI Interface (SPI) • Updated the original Section USB • Updated Section 4.13 PWM Groups (PWMG) • Updated Section 4.16 Timer Groups (TIMG) • Updated Section 4.17 Watchdog Timers (WDT) • Updated Section 4.18 Real-time Counter (RTC) • Add parameter VDDRAM to Section 5.1 Absolute Maximum Ratings and Section 5.3 Recommended Operating Conditions • Updated storage temperature range in Section 5.1 Absolute Maximum Ratings • Removed Section BUCKPA from Section 5 Electrical Characteristics

Version	Date	Description
		• Updated WLAN TX power in Section 5.15 WLAN RF Transmitter Characteristics • Updated SAR ADC characteristics values in Section 5.18 AUX ADC Characteristics
1.2	2023/3/31	Removed 802.11ac support
1.3	2023/6/9	• Renamed some interfaces and peripherals • Updated Section 1 Features • Updated Section 2 Overview • Updated pin assignments and pin description for QFN40 package in Section 3 Pin Descriptions • Updated Section 4 Functional Description • Updated and added measurement data in Section 5 Electrical Characteristics • Added Section 5.2 ESD Ratings and Section 5.4 Digital I/O Characteristics
1.4	2023/6/16	• Updated dual-mode Bluetooth support to Bluetooth Low Energy support • Updated core description
1.5	2023/9/25	• General wording fixes • Updated OFDMA and TWT support and added Bluetooth LE features in Section 1 Features • Renamed low-voltage sleep mode to sleep mode and removed normal sleep mode throughout document • Updated pin assignments for QFN40 package • Corrected pin assignments for UART0 CTS and RTS in Section 3 Pin Descriptions • Updated Section 4.2 Clock Management • Added FIFO feature for IrDA interface in Section 4.19 IrDA Interface (IrDA) • Corrected absolute max. ratings for VDDD and VDDDIG in Section 5.1 Absolute Maximum Ratings • Updated ordering information in Section 8 Ordering Information
1.6	2023/12/13	• Updated QFN40 pin assignments: updated the number of I2C interfaces, PWM channels, ADC channels, and touch sensing I/Os, and removed DISPLAY controller and CLK26M clock signal • Updated Wi-Fi RX sensitivity, and updated and added current values in Section 1 Features • Updated Section 3 Pin Descriptions • Updated the note on selecting bypass capacitors in Section 4.4.1

Version	Date	Description
		Power Scheme • Updated the description of PWM channels in Section 4.13 PWM Groups (PWMG) • Removed note “Values currently listed in this section are preliminary measurements and are subject to change.” from Section 5 Electrical Characteristics • Added VBAT slew rate to Section 5.3 Recommended Operating Conditions • Updated and added current values in Section 5.13 Current Consumption • Updated and added RF characteristic values in Section 5.14 WLAN RF Receiver Characteristics to Section 5.17 Bluetooth LE RF Transmitter Characteristics • Updated QFN40 package outline and mechanical specifications in Section 6 Package Information • Updated RoHS compliance statement in Section 7 Reflow Soldering Profile
1.7	2024/5/11	• Updated Wi-Fi operating mode support, updated maximum VBAT voltage, and updated current for sleep and deep sleep modes in Section 1 Features • Updated core name • Removed 32.768 kHz crystal oscillator from the document • Corrected GDMA channel number • Updated maximum operating temperature • Updated the description of Section 4.3 Reset • Updated voltage ranges for VBAT, VDDA, VDDD, and VDDRAM in Figure 4-1, updated Figure 4-2 and Table 4-1, and added Figure 4-3 and Table 4-2 in Section 4.4.1 Power Scheme • Updated UART baud rate in Section 4.7 UART Interfaces (UART) • Updated SDIO clock frequency in Section 4.8 SDIO Interface (SDIO) • Added I2C FIFO feature in Section 4.9 I2C Interface (I2C) • Updated the description of Section 4.13 PWM Groups (PWMG) • Updated the introduction to IrDA interface in Section 4.19 IrDA Interface (IrDA) • Updated maximum voltages for power supplies in Section 5.1 Absolute Maximum Ratings • Added notes and updated voltage ranges for VBAT, VDDA, VDDD, and VDDRAM in Section 5.3 Recommended Operating Conditions • Added Section 5.5 IO LDO • Updated VDDA (LDO output) minimum and maximum voltages in

Version	Date	Description
		Section 5.6 Analog LDO • Updated VDDA (buck output) minimum voltage and minimum inductor saturation current in Section 5.10 Analog Buck • Updated maximum load capacitance of the 26 MHz crystal in Section 5.12 26 MHz Crystal Characteristics • Updated and added current for active mode and sleep modes in Section 5.13 Current Consumption • Updated ordering code in Section 8 Ordering Information
1.8	2024/9/5	• General wording fixes • Updated operating voltage range • Renamed pin # 2 of the QFN40 package • Updated the description of Section 4.1 Wi-Fi/Bluetooth Transceiver • Updated the description of Section 4.3 Reset • Updated VIO description, Figure 4-1, and power-up sequence timing parameter T_4 values in Section 4.4.1 Power Scheme • Updated the description of sleep mode in Section 4.4.2 Power Modes • Corrected maximum sampling rate and VBAT monitoring channel input voltage for AUX ADC in Section 4.15 Auxiliary ADC (AUX ADC) • Updated maximum voltages for VBAT, SWA, and SWD in Section 5.1 Absolute Maximum Ratings • Added HBM and CDM values in Section 5.2 ESD Ratings • Updated the voltages of VBAT, VCCIF, VCCRXFE, VCCPLL, VCCA, VDDA, VDDD, and VDDDIG in Section 5.3 Recommended Operating Conditions • Updated VIO typical voltage in Section 5.5 IO LDO • Updated VDDA (LDO output) voltage in Section 5.6 Analog LDO • Updated VDDD (LDO output) voltage in Section 5.7 Digital LDO • Updated VDDDIG voltage in Section 5.8 Core LDO • Updated VDDA (buck output) voltage in Section 5.10 Analog Buck • Updated VDDD (buck output) voltage in Section 5.11 Digital Buck • Added minimum conversion clock frequency, and updated V_{REF} and input voltage range for AUX ADC in Section 5.18 AUX ADC Characteristics
1.9	2025/4/3	• Section 1 Features: – Added flash XIP support – Added packaging information of BK7236QH4068 • Updated Figure 4-1 Internal Power Distribution in Section 4.4.1 Power Scheme

Version	Date	Description
		• Updated the minimum value of VOH in Section 5.4 Digital I/O Characteristics • Added Section 6.2 QFN40 5 x 5 x 0.9 mm Package • Section 8 Ordering Information: – Updated the title of Figure 8-1 – Added a note about MOQ in Table 8-1 – Added ordering code BK7236QH4068 in Table 8-1
2.0	2025/6/16	• Added BK7236QH4150 QFN40 package information • Added two footnotes regarding the usage of specific GPIOs to Table 3-3 Pin Multiplexing in Section 3.3 Pin Multiplexing • Removed maximum values for power-up sequence timing parameter T_2 and T_3 in Table 4-1 Timing Parameters of Power-up Sequence in Section 4.4.1 Power Scheme • Modified the description of wake-up sources for deep sleep and sleep modes in Section 4.4.2 Power Modes • Added Section 5.9 EXMEM LDO • Added adjacent channel rejection values for IEEE 802.11n and IEEE 802.11ax in Section 5.14 WLAN RF Receiver Characteristics • Added Intermodulation values for Bluetooth LE 1 Mbps and 2 Mbps in Section 5.16 Bluetooth LE RF Receiver Characteristics

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