BK7252N Datasheet

DS-BK7252N-E01 V1.0

2025/6/11

IP Camera

- DTIM10 250 μA
- 200 mA battery charger

Endoscope

- 720p resolution
- 544 KB RAM for smooth and clear image transfer

Drone

- SPI interfaces and DVP interface for dual cameras
- 720p resolution

Dashcam

- 720p at 30 fps
- 120 MHz QSPI interface for display

Contents

1. Features

Wi-Fi®

- IEEE 802.11b/g/n 1x1 compliant
- Supports 20 MHz channel
- STBC supported
- Supports STA and SoftAP modes
- Supports concurrent SoftAP + STA
- TX power up to +17.5 dBm
- RX sensitivity -98 dBm

Bluetooth® Low Energy

- Bluetooth Low Energy (LE) 5.2
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: 2 Mbps, advertising extensions, and long range

Core

- 32-bit MCU at up to 160 MHz
- UART flash download
- SPI flash download
- JTAG debug interface

Memories

- SiP flash up to 4 MB
- On-chip 544 KB RAM
- 4-byte eFuse

Clock Management

- External oscillators: 26 MHz crystal oscillator (XTALH), 32 kHz crystal oscillator (XTALL) (QFN40)
- Internal oscillators: 26–160 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 480 MHz PLL (DPLL)

Power Management

- 2.7 to 4.35 V VCCBAT supply

- 4.3 to 5.5 V VCCUSB supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded LDO regulators
- 200 mA battery charger
- Low power consumption:
  - Active mode RX: 42 mA
  - Active mode TX @ 17 dBm: 330 mA
  - Sleep mode: 90 µA
  - Shutdown mode: 1 µA

Peripherals

- GPIOs: 38 in QFN68, 29 in QFN48, 27 in QFN40
- 2x SPI: 1 supports master and slave modes, 1 supports slave mode
- 1x QSPI
- 3x UART, 1 with hardware flow control and flash download support
- 1x SDIO
- 2x I2C
- 1x general-purpose DMA controller (GDMA) with 8 channels
- 1x JPEG hardware encoder
- 1x 8-bit CIS DVP interface
- 6x 32-bit PWM channel
- 1x I2S
- 1x four-band digital hardware equalizer
- 1x audio ADC
- 1x audio DAC
- 10-bit AUX ADC, up to 7 channels
- 6x 32-bit general-purpose timer
- 1x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x IrDA
- 1x temperature sensor
- 1x true random number generator (TRNG)

Packaging

- QFN68 package, 8 x 8 mm
- QFN48 package, 6 x 6 mm
- QFN40 package, 5 x 5 mm
- Operating temperature range: -40 to +85 °C

Applications

- Home appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart plug
- Smart lighting
  - Light bulb
  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

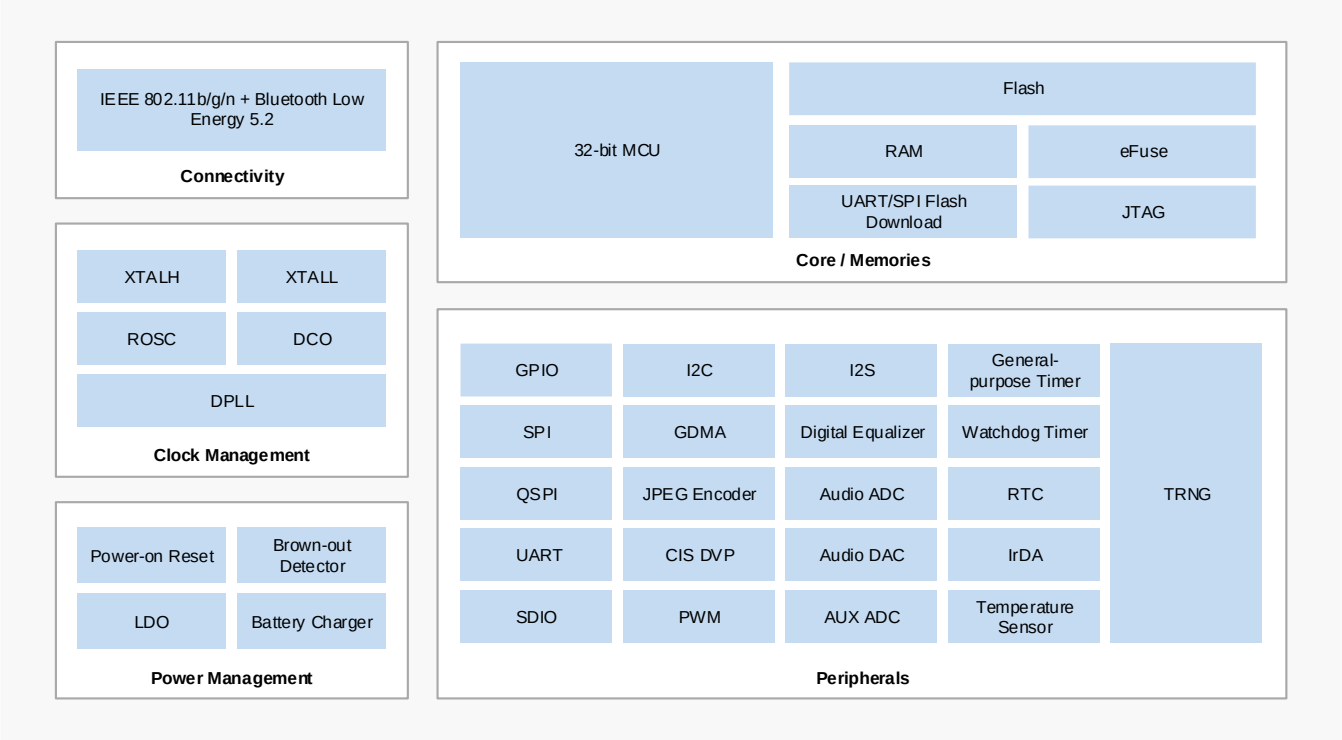
2. Overview

The BK7252N is a highly integrated single-chip Wi-Fi 802.11b/g/n and Bluetooth Low Energy (LE) 5.2 combo solution designed for applications that require low power consumption and abundant resources. The integration of a powerful 32-bit MCU and a comprehensive set of peripherals and interfaces makes the BK7252N ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and process technology, the BK7252N delivers high integration and minimal power consumption for IP cameras, endoscopes, drones, dashcams, and other advanced IoT and automotive applications.

Figure 2-1 shows the general block diagram of the BK7252N.

Figure 2-1 BK7252N Block Diagram



The BK7252N devices are offered in three packages. The set of included peripherals varies depending on the package. Table 2-1 shows the list of peripherals available on each package.

Table 2-1 Device Options and Features

Feature	QFN68	QFN48	QFN40
SiP flash	2 MB or 4 MB	2 MB or 4 MB	1 MB or 2 MB

Feature		QFN68	QFN48	QFN40
GPIO		38	29	27
SPI	Master/Slave	1	1	1
	Slave	1	1	1
QSPI		1	-	-
UART		3	2	2 (hardware flow control not supported)
SDIO		1	1	1
I2C	Master/Slave	2	2	2
GDMA		1	1	1
JPEG encoder		1	1	1
CIS DVP interface		1	1	1
PWM	PWM0–5	4	1	2
I2S	Master/Slave	1	-	-
Digital equalizer		1	1	1
Audio ADC		1	1	-
Audio DAC		Mono	Mono	-
AUX ADC	10 bits	1	1	1
	Number of channels	7	6	4
General-purpose timer		6	6	6
Watchdog timer		1	1	1
Real-time counter		1	1	1
IrDA		1	-	-
Temperature sensor		1	1	1
TRNG		1	1	1
Package		8 x 8 mm QFN68	6 x 6 mm QFN48	5 x 5 mm QFN40
Operating voltage		2.7 to 4.35 V or 4.3 to 5.5 V	2.7 to 4.35 V or 4.3 to 5.5 V	2.7 to 4.35 V
Operating temperature		-40 to +85 °C		

3. Pin Descriptions

The BK7252N provides Wi-Fi and Bluetooth LE functionality in three packages of 40 pins, 48 pins, and 68 pins.

3.1 QFN68 Pin Descriptions

Figure 3-1 shows the pin assignments of the 8 x 8 mm, 68-pin QFN package.

Figure 3-1 QFN68 Pin Assignments

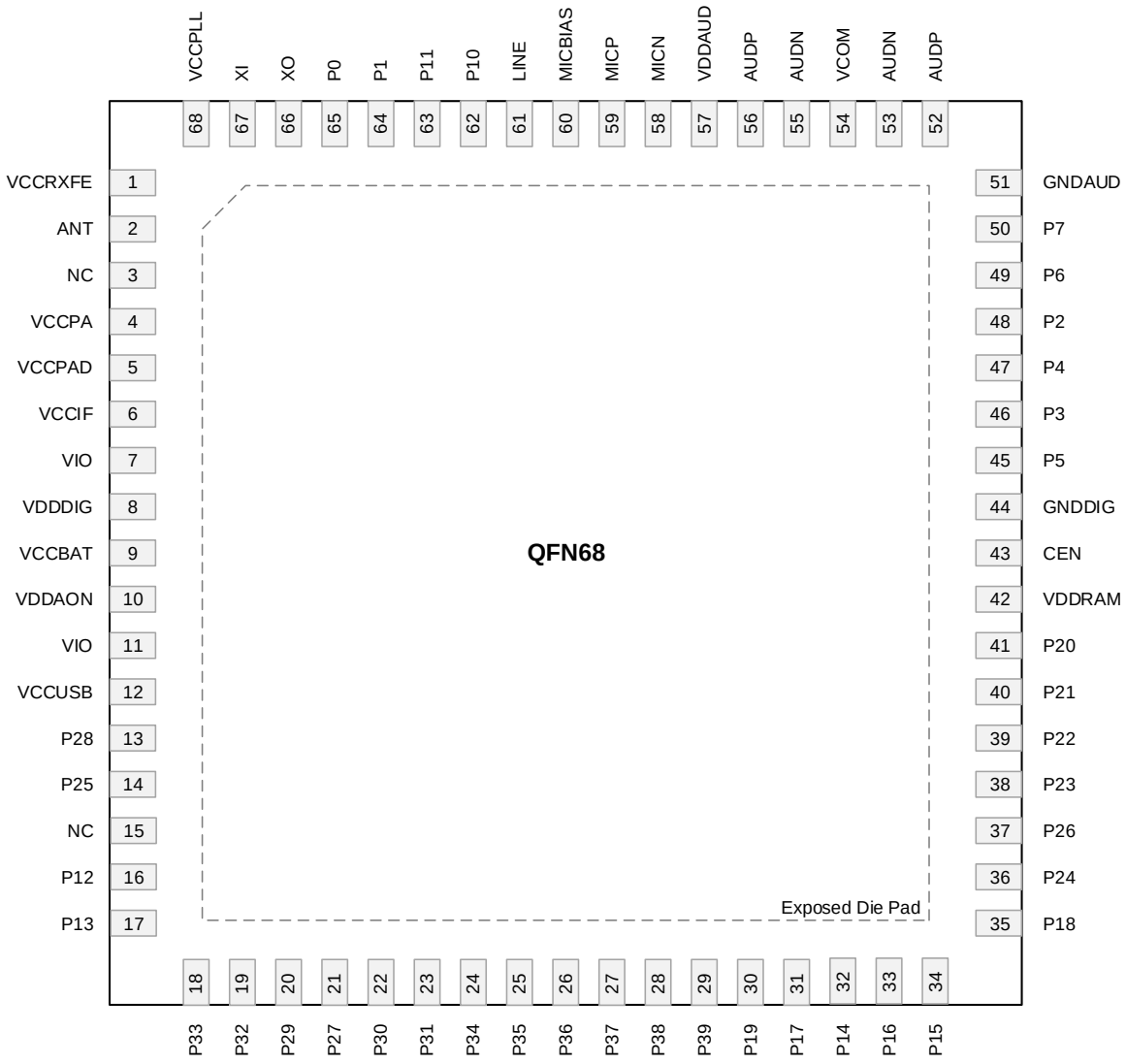


Table 3-1 shows the pin descriptions of the QFN68 package.

Table 3-1 QFN68 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	NC	-	NC	No connect
4	VCCPA	-	Analog input	RF PA power supply
5	VCCPAD	-	Analog input	RF PA driver power supply
6	VCCIF	-	Analog input	IF power supply
7	VIO	-	Analog output	IO LDO output
8	VDDDIG	-	Analog output	Digital LDO output
9	VCCBAT	-	Power	Chip power supply
10	VDDAON	-	Analog output	Always-on LDO output
11	VIO	-	Analog output	IO LDO output
12	VCCUSB	-	Power	Chip power supply
13	P28	I/O	Digital	• GPIO28: general-purpose I/O • RX_EN: RX enable
14	P25	I/O	Digital	• GPIO25: general-purpose I/O • TX_EN: TX enable
15	NC	-	NC	No connect
16	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • UART0_RTS: request to send • ADC6: analog input channel
17	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O • UART0_CTS: clear to send • ADC7: analog input channel
18	P33	I/O	Digital	• GPIO33: general-purpose I/O • CIS_PXD1: data • SPI0/1_MISO: master in slave out
19	P32	I/O	Digital	• GPIO32: general-purpose I/O • CIS_PXD0: data • SPI0/1_MOSI: master out slave in

Pin #	Name	I/O	Type	Description
20	P29	I/O	Digital	• GPIO29: general-purpose I/O • CIS_PCLK: pixel clock
21	P27	I/O	Digital	• GPIO27: general-purpose I/O • CIS_MCLK: master clock
22	P30	I/O	Digital	• GPIO30: general-purpose I/O • CIS_HSYNC: horizontal synchronization • SPI0/1_SCK: serial clock
23	P31	I/O	Digital	• GPIO31: general-purpose I/O • CIS_VSYNC: vertical synchronization • SPI0/1_CSN: chip select
24	P34	I/O	Digital	• GPIO34: general-purpose I/O • CIS_PXD2: data • SD_CLK: clock
25	P35	I/O	Digital	• GPIO35: general-purpose I/O • CIS_PXD3: data • SD_CMD: command/response
26	P36	I/O	Digital	• GPIO36: general-purpose I/O • CIS_PXD4: data • SD_DATA0: data
27	P37	I/O	Digital	• GPIO37: general-purpose I/O • CIS_PXD5: data • SD_DATA1: data
28	P38	I/O	Digital	• GPIO38: general-purpose I/O • CIS_PXD6: data • SD_DATA2: data
29	P39	I/O	Digital	• GPIO39: general-purpose I/O • CIS_PXD7: data • SD_DATA3: data
30	P19	I/O	Digital	• GPIO19: general-purpose I/O • SD_DATA1: data • QSPI_IO3: data
31	P17	I/O	Digital	• GPIO17: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• SD_DATA0: data • SPI0/1_MISO: master in slave out • QSPI_IO1: data
32	P14	I/O	Digital	• GPIO14: general-purpose I/O • SD_CLK: clock • SPI0/1_SCK: serial clock
33	P16	I/O	Digital	• GPIO16: general-purpose I/O • SD_CMD: command/response • SPI0/1_MOSI: master out slave in • QSPI_IO0: data
34	P15	I/O	Digital	• GPIO15: general-purpose I/O • SD_DATA3: data • SPI0/1_CSN: chip select
35	P18	I/O	Digital	• GPIO18: general-purpose I/O • SD_DATA2: data • QSPI_IO2: data
36	P24	I/O	Digital	• GPIO24: general-purpose I/O • LPO_CLK: 32 kHz clock output • PWM4 (differential with PWM5) • QSPI_CLK: serial clock
37	P26	I/O	Digital	• GPIO26: general-purpose I/O • IRDA: infrared data • PWM5 (differential with PWM4) • QSPI_CSN: chip select
38	P23	I/O	Digital	• GPIO23: general-purpose I/O • DL_SPI_SO: SPI Flash download slave out • ADC3: analog input channel • JTAG_TDO: test data output • QSPI_IO0: data
39	P22	I/O	Digital	• GPIO22: general-purpose I/O • DL_SPI_SI: SPI Flash download slave in • CLK26M: 26 MHz clock output

Pin #	Name	I/O	Type	Description
				• JTAG_TDI: test data input • QSPI_IO1: data
40	P21	I/O	Digital	• GPIO21: general-purpose I/O • DL_SPI_CSN: SPI Flash download chip select • I2C0_SDA: serial data • JTAG_TMS: test mode select • QSPI_IO2: data
41	P20	I/O	Digital	• GPIO20: general-purpose I/O • DL_SPI_SCK: SPI Flash download serial clock • I2C0_SCL: serial clock • JTAG_TCK: test clock • QSPI_IO3: data
42	VDDRAM	-	Analog output	Power supply for PSRAM
43	CEN	-	Analog input	Chip enable, active high
44	GNDDIG	-	GND	Ground
45	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • I2S_DOUT: serial data output • ADC2: analog input channel
46	P3	I/O	Digital/Analog	• GPIO3: general-purpose I/O • I2S_SYNC: frame synchronization • ADC5: analog input channel • UART2_RX: receive data input
47	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O • I2S_DIN: serial data input • ADC1: analog input channel
48	P2	I/O	Digital/Analog	• GPIO2: general-purpose I/O • I2S_CLK: serial clock • ADC4: analog input channel • UART2_TX: transmit data output
49	P6	I/O	Digital	• GPIO6: general-purpose I/O • CLK13M: 26 MHz clock output (divide by 1/2/4/8)

Pin #	Name	I/O	Type	Description
				• PWM0 (differential with PWM1)
50	P7	I/O	Digital	• GPIO7: general-purpose I/O • PWM1 (differential with PWM0)
51	GNDAUD	-	GND	Ground
52	AUDP	-	Analog output	Audio positive output
53	AUDN	-	Analog output	Audio negative output
54	VCOM	-	Analog output	Common mode output
55	AUDN	-	Analog output	Audio negative output
56	AUDP	-	Analog output	Audio positive output
57	VDDAUD	-	Analog output	Audio LDO output
58	MICN	-	Analog input	Microphone negative input
59	MICP	-	Analog input	Microphone positive input
60	MICBIAS	-	Analog output	Microphone bias output
61	LINE	-	Analog input	Line in input
62	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART Flash download receive data input • UART0_RX: receive data input
63	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART Flash download transmit data output • UART0_TX: transmit data output
64	P1	I/O	Digital	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data
65	P0	I/O	Digital	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock
66	XO	-	Analog output	26 MHz crystal output
67	XI	-	Analog input	26 MHz crystal input
68	VCCPLL	-	Analog input	RF PLL power supply

Pin #	Name	I/O	Type	Description
Die pad	GND_SLUG	-	GND	Ground

3.2 QFN48 Pin Descriptions

Figure 3-2 shows the pin assignments of the 6 x 6 mm, 48-pin QFN package.

Figure 3-2 QFN48 Pin Assignments

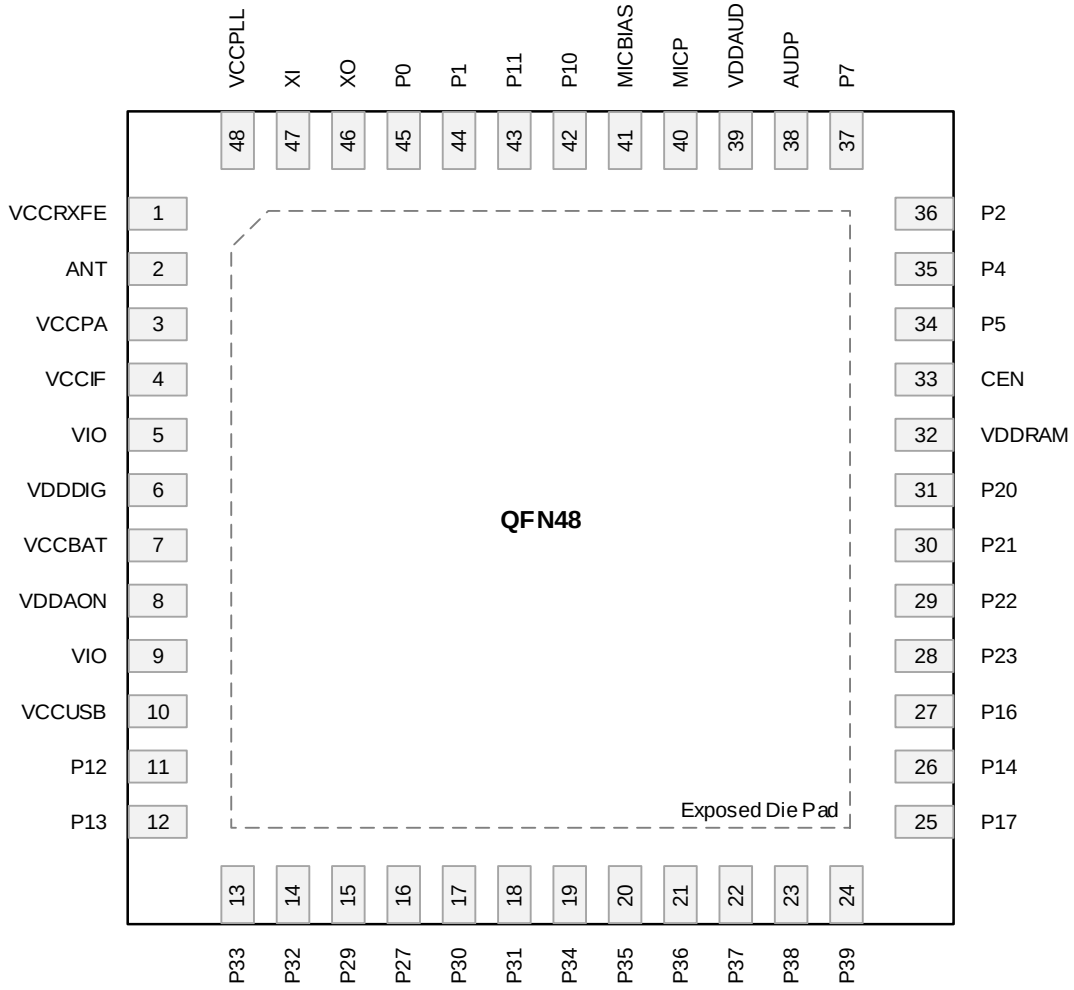


Table 3-2 shows the pin descriptions of the QFN48 package.

Table 3-2 QFN48 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCIF	-	Analog input	IF power supply
5	VIO	-	Analog output	IO LDO output
6	VDDDIG	-	Analog output	Digital LDO output
7	VCCBAT	-	Power	Chip power supply
8	VDDAON	-	Analog output	Always-on LDO output
9	VIO	-	Analog output	IO LDO output
10	VCCUSB	-	Power	Chip power supply
11	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • UART0_RTS: request to send • ADC6: analog input channel
12	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O • UART0_CTS: clear to send • ADC7: analog input channel
13	P33	I/O	Digital	• GPIO33: general-purpose I/O • CIS_PXD1: data • SPI0/1_MISO: master in slave out
14	P32	I/O	Digital	• GPIO32: general-purpose I/O • CIS_PXD0: data • SPI0/1_MOSI: master out slave in
15	P29	I/O	Digital	• GPIO29: general-purpose I/O • CIS_PCLK: pixel clock
16	P27	I/O	Digital	• GPIO27: general-purpose I/O • CIS_MCLK: master clock
17	P30	I/O	Digital	• GPIO30: general-purpose I/O • CIS_HSYNC: horizontal synchronization • SPI0/1_SCK: serial clock

Pin #	Name	I/O	Type	Description
18	P31	I/O	Digital	• GPIO31: general-purpose I/O • CIS_VSYNC: vertical synchronization • SPI0/1_CSN: chip select
19	P34	I/O	Digital	• GPIO34: general-purpose I/O • CIS_PXD2: data • SD_CLK: clock
20	P35	I/O	Digital	• GPIO35: general-purpose I/O • CIS_PXD3: data • SD_CMD: command/response
21	P36	I/O	Digital	• GPIO36: general-purpose I/O • CIS_PXD4: data • SD_DATA0: data
22	P37	I/O	Digital	• GPIO37: general-purpose I/O • CIS_PXD5: data • SD_DATA1: data
23	P38	I/O	Digital	• GPIO38: general-purpose I/O • CIS_PXD6: data • SD_DATA2: data
24	P39	I/O	Digital	• GPIO39: general-purpose I/O • CIS_PXD7: data • SD_DATA3: data
25	P17	I/O	Digital	• GPIO17: general-purpose I/O • SD_DATA0: data • SPI0/1_ MISO: master in slave out
26	P14	I/O	Digital	• GPIO14: general-purpose I/O • SD_CLK: clock • SPI0/1_SCK: serial clock
27	P16	I/O	Digital	• GPIO16: general-purpose I/O • SD_CMD: command/response • SPI0/1_MOSI: master out slave in
28	P23	I/O	Digital	• GPIO23: general-purpose I/O • DL_SPI_SO: SPI Flash download slave out

Pin #	Name	I/O	Type	Description
				• ADC3: analog input channel • JTAG_TDO: test data output
29	P22	I/O	Digital	• GPIO22: general-purpose I/O • DL_SPI_SI: SPI Flash download slave in • CLK26M: 26 MHz clock output • JTAG_TDI: test data input
30	P21	I/O	Digital	• GPIO21: general-purpose I/O • DL_SPI_CSN: SPI Flash download chip select • I2C0_SDA: serial data • JTAG_TMS: test mode select
31	P20	I/O	Digital	• GPIO20: general-purpose I/O • DL_SPI_SCK: SPI Flash download serial clock • I2C0_SCL: serial clock • JTAG_TCK: test clock
32	VDDRAM	-	Analog output	Power supply for PSRAM
33	CEN	-	Analog input	Chip enable, active high
34	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • ADC2: analog input channel
35	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O • ADC1: analog input channel
36	P2	I/O	Digital/Analog	• GPIO2: general-purpose I/O • ADC4: analog input channel
37	P7	I/O	Digital	• GPIO7: general-purpose I/O • PWM1
38	AUDP	-	Analog output	Audio positive output
39	VDDAUD	-	Analog output	Audio LDO output
40	MICP	-	Analog input	Microphone positive input
41	MICBIAS	-	Analog output	Microphone bias output
42	P10	I/O	Digital	• GPIO10: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• DL_UART_RX：UART Flash download receive data input • UART0_RX: receive data input
43	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX：UART Flash download transmit data output • UART0_TX: transmit data output
44	P1	I/O	Digital	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data
45	P0	I/O	Digital	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock
46	XO	-	Analog output	26 MHz crystal output
47	XI	-	Analog input	26 MHz crystal input
48	VCCPLL	-	Analog input	RF PLL power supply
Die pad	GND_SLUG	-	GND	Ground

3.3 QFN40 Pin Descriptions

Figure 3-3 shows the pin assignments of the 5 x 5 mm, 40-pin QFN package.

Figure 3-3 QFN40 Pin Assignments

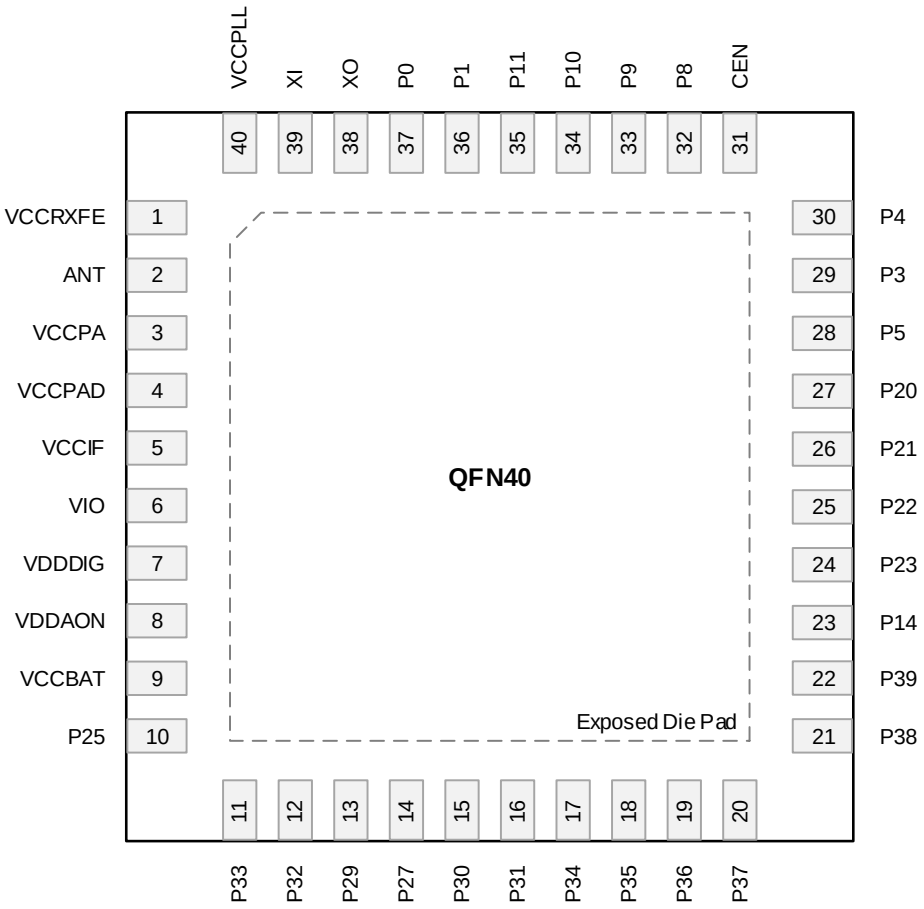


Table 3-3 shows the pin descriptions of the QFN40 package.

Table 3-3 QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCPAD	-	Analog input	RF PA driver power supply
5	VCCIF	-	Analog input	IF power supply
6	VIO	-	Analog output	IO LDO output
7	VDDDIG	-	Analog output	Digital LDO output
8	VDDAON	-	Analog output	Always-on LDO output

Pin #	Name	I/O	Type	Description
9	VCCBAT	-	Power	Chip power supply
10	P25	I/O	Digital	GPIO25: general-purpose I/O
11	P33	I/O	Digital	• GPIO33: general-purpose I/O • CIS_PXD1: data • SPI0/1_MISO: master in slave out
12	P32	I/O	Digital	• GPIO32: general-purpose I/O • CIS_PXD0: data • SPI0/1_MOSI: master out slave in
13	P29	I/O	Digital	• GPIO29: general-purpose I/O • CIS_PCLK: pixel clock
14	P27	I/O	Digital	• GPIO27: general-purpose I/O • CIS_MCLK: master clock
15	P30	I/O	Digital	• GPIO30: general-purpose I/O • CIS_HSYNC: horizontal synchronization • SPI0/1_SCK: serial clock
16	P31	I/O	Digital	• GPIO31: general-purpose I/O • CIS_VSYNC: vertical synchronization • SPI0/1_CSN: chip select
17	P34	I/O	Digital	• GPIO34: general-purpose I/O • CIS_PXD2: data • SD_CLK: clock
18	P35	I/O	Digital	• GPIO35: general-purpose I/O • CIS_PXD3: data • SD_CMD: command/response
19	P36	I/O	Digital	• GPIO36: general-purpose I/O • CIS_PXD4: data • SD_DATA0: data
20	P37	I/O	Digital	• GPIO37: general-purpose I/O • CIS_PXD5: data • SD_DATA1: data
21	P38	I/O	Digital	• GPIO38: general-purpose I/O • CIS_PXD6: data

Pin #	Name	I/O	Type	Description
				• SD_DATA2: data
22	P39	I/O	Digital	• GPIO39: general-purpose I/O • CIS_PXD7: data • SD_DATA3: data
23	P14	I/O	Digital	• GPIO14: general-purpose I/O • SD_CLK: clock • SPI0/1_SCK: serial clock
24	P23	I/O	Digital	• GPIO23: general-purpose I/O • DL_SPI_SO: SPI Flash download slave out • ADC3: analog input channel • JTAG_TDO: test data output
25	P22	I/O	Digital	• GPIO22: general-purpose I/O • DL_SPI_SI: SPI Flash download slave in • CLK26M: 26 MHz clock output • JTAG_TDI: test data input
26	P21	I/O	Digital	• GPIO21: general-purpose I/O • DL_SPI_CSN: SPI Flash download chip select • I2C0_SDA: serial data • JTAG_TMS: test mode select
27	P20	I/O	Digital	• GPIO20: general-purpose I/O • DL_SPI_SCK: SPI Flash download serial clock • I2C0_SCL: serial clock • JTAG_TCK: test clock
28	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • ADC2: analog input channel
29	P3	I/O	Digital/Analog	• GPIO3: general-purpose I/O • ADC5: analog input channel
30	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O • ADC1: analog input channel
31	CEN	-	Analog input	Chip enable, active high

Pin #	Name	I/O	Type	Description
32	P8	I/O	Digital/Analog	• GPIO8: general-purpose I/O • PWM2 (differential with PWM3) • 32K_XI: 32.768 kHz crystal input
33	P9	I/O	Digital/Analog	• GPIO9: general-purpose I/O • PWM3 (differential with PWM2) • 32K_XO: 32.768 kHz crystal output
34	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART Flash download receive data input • UART0_RX: receive data input
35	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART Flash download transmit data output • UART0_TX: transmit data output
36	P1	I/O	Digital	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data
37	P0	I/O	Digital	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock
38	XO	-	Analog output	26 MHz crystal output
39	XI	-	Analog input	26 MHz crystal input
40	VCCPLL	-	Analog input	RF PLL power supply
Die pad	GND_SLUG	-	GND	Ground

4. Functional Description

4.1 Wi-Fi/Bluetooth Transceiver

The BK7252N integrates a high-performance Wi-Fi/Bluetooth transceiver. The transceiver incorporates two on-chip baluns. On the receive side, the on-chip balun converts the single-ended (unbalanced) RF signal from the antenna into a differential (balanced) signal and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the on-chip balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with only one ANT pin connected to the antenna. The communication range can be extended by configuring GPIO25 and GPIO28 as TX_EN and RX_EN function to control external PA and LNA. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Clock Management

The primary clock sources available in the BK7252N are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator (XTALH)
  - 26–160 MHz internal digitally controlled oscillator (DCO)
  - 480 MHz digital PLL (DPLL)
- Low-frequency clock
  - 32 kHz internal ring oscillator (ROSC)
  - 32 kHz (32.768 kHz) crystal oscillator (XTALL) (QFN40)

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz clock signal derived from 26 MHz crystal oscillator
- 32 kHz internal oscillator ROSC
- 32 kHz crystal oscillator XTALL (QFN40)

The BK7252N also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- CLK26M: high-frequency crystal clock, generally 26 MHz
- CLK13M: clock derived from 26 MHz crystal clock (factor 1/2/4/8)

- LPO_CLK: LPO_CLK clock
- CIS_MCLK: reference clock for external CMOS image sensor (CIS)

4.3 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

Power-on reset, brown-out reset, and watchdog reset have the same reset effect on all blocks, except for the always-on logic. Any of these three resets can reset the whole chip to its initial state. The always-on logic has a 64-bit timer and a 16-bit retention register, which can only be reset to initial values by a power-on reset or brown-out reset.

Wake-up from shutdown mode triggers the whole system reset, while wake-up from deep sleep mode triggers the reset of digital blocks.

4.4 Power Management

4.4.1 Power Scheme

The power management system on the BK7252N includes several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The chip can be powered by 2.7 to 4.35 V VCCBAT or 4.3 to 5.5 V VCCUSB. The VCCBAT or VCCUSB generates VIO through the IO LDO regulator. VIO is the input supply of other LDOs.

When only VCCBAT is present, the IO LDO regulator is powered by VCCBAT. Similarly, when only VCCUSB is present, the IO LDO regulator is powered by VCCUSB. If both VCCBAT and VCCUSB are present, the IO LDO regulator is powered by VCCUSB when VCCBAT is below 3.0 V, and by VCCBAT when VCCBAT is above 3.0 V.

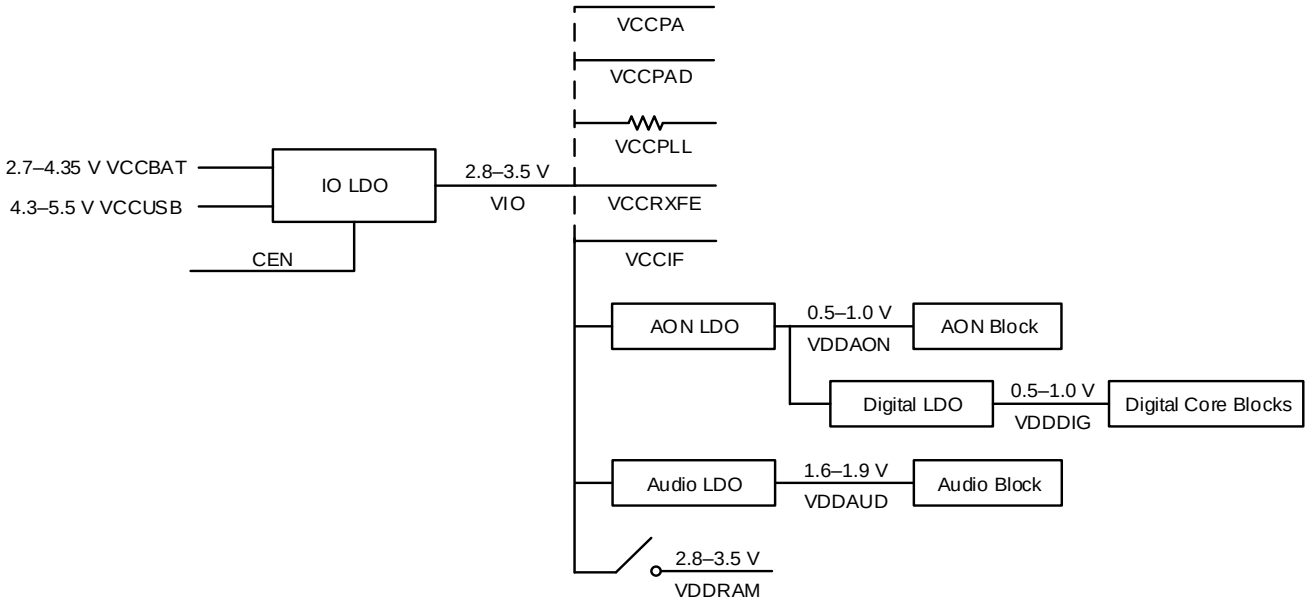
The LDOs generate the following main power supplies:

- VIO: power supply for RF and analog blocks as well as PSRAM.
  - It is externally connected to VCCPA, VCCPAD, VCCPLL, VCCRXFE, and VCCIF to supply power to the Wi-Fi/Bluetooth transceiver, and internally provides power to DPLL, XTAL, AUX ADC, and AUDIO directly.
  - It is connected to VDDRAM through a switch to supply power to PSRAM.
- VDDDIG: power supply for digital domain. It provides power supply for the processor, memory, Wi-Fi and Bluetooth basebands, as well as various peripherals.

- VDDAON: power supply for always-on (AON) domain. The AON block, including RTC and control logic of deep sleep wake-up, keeps working in deep sleep mode (VDDDIG off).
- VDDAUD: power supply for audio block.

Figure 4-1 shows the power distribution of the BK7252N.

Figure 4-1 Internal Power Distribution



Note: Outputs from the LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-2 shows the power-up sequence of the BK7252N.

Figure 4-2 BK7252N Power-up Sequence

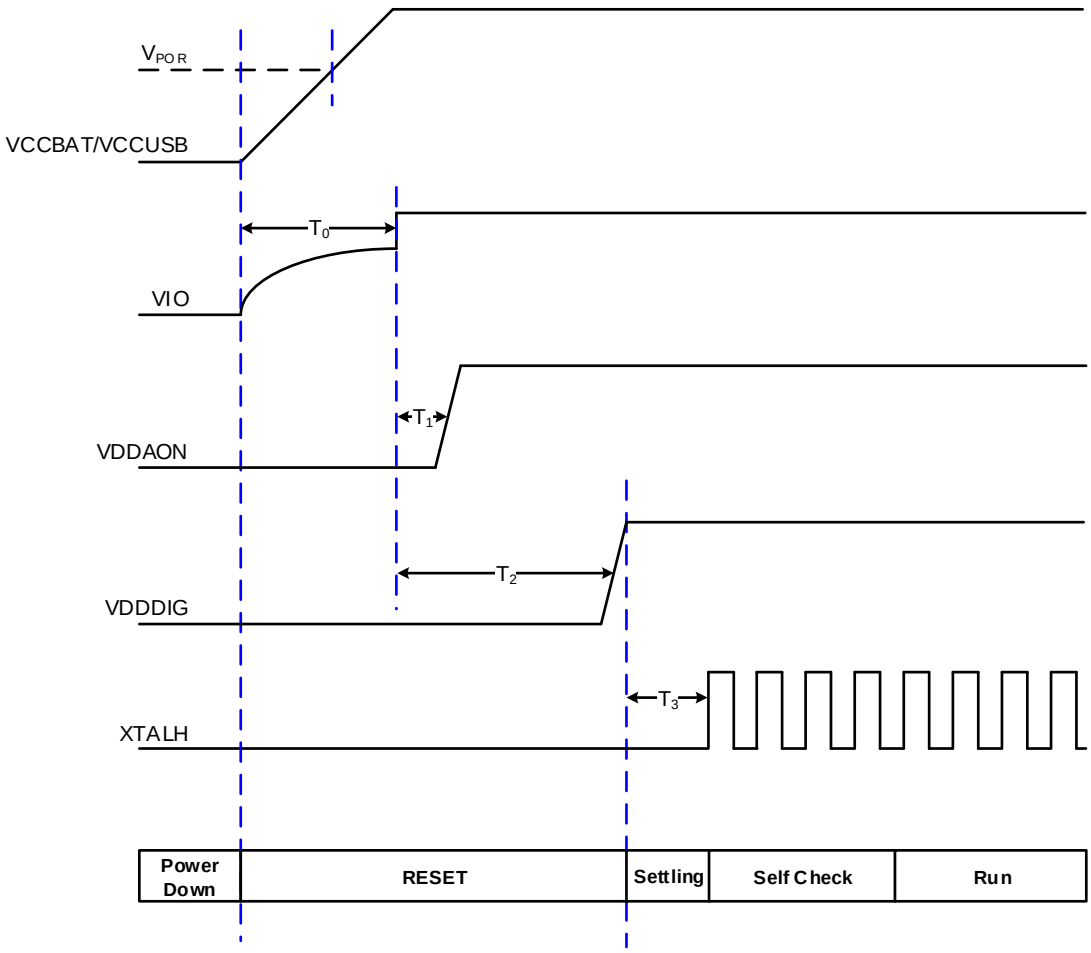


Table 4-1 Timing Parameters of Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{POR}	VCCBAT POR threshold	-	2	-	V
	VCCUSB POR threshold	-	4	-	V
T_0	IO LDO output ready time, supplied by VCCBAT	-	2	-	ms
	IO LDO output ready time, supplied by VCCUSB		1.6		ms
T_1	AON LDO output ready time	-	0.4	-	ms
T_2	Digital LDO output ready time	-	3	-	ms
T_3	XTALH stable time	-	1.2	-	ms

4.4.2 Battery Charger

When VCCUSB is above 4.3 V, the external battery connected to VCCBAT can be charged through the battery charger.

The battery charger supports 200 mA constant current charging. Charging current can be programmed in 1.5 mA/step. When the battery reaches the desired voltage threshold, the charger switches to constant voltage charging mode.

4.4.3 Power Modes

The BK7252N supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the AON block. A GPIO event or an RTC event can power up the system again. The retention register holds its content.

Sleep Mode: The MCU and all digital blocks stop their clocks. A charger event, a GPIO event, an RTC event, a Wi-Fi MAC counter event, or a Bluetooth MAC counter event can bring the system back to active mode with normal voltage.

Active Mode: The MCU is active, and all peripherals are available.

4.5 General-purpose I/Os (GPIO)

The BK7252N has up to 40 GPIOs, which can be configured as either input or output. All GPIOs are shared with alternate functions.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.6 SPI Interfaces (SPI)

The BK7252N integrates two SPI interfaces, SPI0 and SPI1. SPI0 can operate in master or slave mode and allows a clock frequency up to 60 MHz in both master and slave modes. SPI1 supports only slave mode and allows a clock frequency up to 60 MHz. SPI0 and SPI1 share SPI pins.

The SPI interfaces support the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Data width:
  - SPI0: configurable 8-bit or 16-bit data width
  - SPI1: 8-bit data width
- Programmable clock polarity and phase (SPI0)
- Programmable data order with MSB-first or LSB-first shifting
- Each embeds a 64-depth RX FIFO and a 64-depth TX FIFO with DMA capability.

4.7 Quad SPI Interface (QSPI)

The BK7252N embeds a Quad SPI interface that provides support for communicating with external flash, PSRAM, or AMOLED display. The QSPI interface allows communicating up to 120 MHz.

The features of the QSPI interface are listed below:

- Single, dual, or quad SPI input/output
- Two functional modes: indirect mode and memory-mapped mode
- Fully programmable opcode and frame format
- Integrated RX FIFO and TX FIFO
- Supports 8, 16, and 32-bit data accesses

4.8 UART Interfaces (UART)

The BK7252N includes three universal asynchronous receiver/transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 4 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)

- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0) (QFN68 and QFN48)
- Flash download (UART0)

4.9 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7252N. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 60 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant
- SDIO card specification version 2.0 compliant
- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 30 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without CPU load

4.10 I2C Interfaces (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7252N embeds two I2C interfaces, which can operate in master or slave mode.

The features of the I2C interfaces are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

4.11 GDMA Controller (GDMA)

The BK7252N has a general-purpose DMA controller (GDMA) with 8 DMA channels to unload CPU activity. The 8 channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controller allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

A selection of peripherals on the BK7252N have DMA capabilities, including UART0, UART1, UART2, SPI0, SDIO, SPI1, JPEG encoder, I2S, AUDIO, and AUX ADC.

4.12 JPEG Encoder

The BK7252N includes a JPEG encoder for encoding JPEG streams. The JPEG encoder provides a small hardware compressor for JPEG images. It supports up to 32 programmable quantization tables.

4.13 CMOS Image Sensor Interface (CIS)

The CMOS Image Sensor (CIS) Digital Video Port (DVP) interface provides an 8-bit parallel interface to sensors, together with master clock (MCLK), pixel clock (PCLK), horizontal SYNC (HSYNC), and vertical SYNC (VSYNC) signals.

The input from the YUV sensor is directly fed to the hardware JPEG encoder, and the output of the JPEG encoder is directly written to the data memory by a dedicated DMA channel.

The CIS interface features include:

- 8-bit parallel interface
- Programmable polarity for pixel clock and synchronization signals
- Crop feature
- Data formats supported:
  - YCbCr 4:2:2 (YUYV, UYVY, YYUV, and UVYY)
  - RGB565

4.14 PWM

The BK7252N has three 32-bit PWM pairs labeled PWM0/1, PWM2/3, and PWM4/5. Each PWM pair consists of two 32-bit up counters driven by an 8-bit programmable prescaler.

Each channel can work independently (arbitrary waveform configuration), or two channels can be paired (waveforms completely opposite, timing aligned).

The PWM features are listed here:

- 32-bit up counter
- The counter increases in one direction and automatically continues counting from 0 when it overflows to the maximum value.
- Fixed PWM base frequency with 8-bit programmable prescaler (factor between 1 and 256)
- Six channels, each supports four modes:
  - PWM mode
  - Timer mode
  - Counter mode
  - Capture mode
- Each channel can be enabled individually, and the mode of each channel can be configured individually.
- Configurable PWM period and duty cycle for each PWM channel
- Capable of continuously counting between two rising edges, two falling edges, or any two edges in Capture mode
- Real-time count value can be read in Timer mode.

4.15 I2S Interface (I2S)

The BK7252N integrates an I2S interface that supports master and slave modes with a sampling rate from 8 kHz to 384 kHz. The I2S interface supports both PCM mono channel and I2S stereo channel modes.

Listed here are the I2S features:

- Master or slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler
- Multiple I2S protocols supported:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Programmable clock polarity
- Integrated 32-bit RX FIFO and 32-bit TX FIFO, both with a depth of 32 x 3 channels

4.16 Audio Peripherals

The BK7252N comes with a rich set of audio peripherals to enhance the listening experience. The chip includes a four-band digital equalizer, an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), a microphone input amplifier and a bias generator, a microphone input, a line-in input, an audio output, etc.

4.16.1 Four-band Digital Equalizer

A dedicated four-band digital equalizer is implemented prior to digital-to-analog conversion, allowing the user to customize the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption.

4.16.2 Audio ADC and DAC

The BK7252N contains a 16-bit ADC with a sampling rate of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates a 16-bit DAC with a sampling rate of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz.

4.16.3 Microphone Input Amplifier and Bias Generator

The BK7252N has a fully differential analog microphone input amplifier and a low-noise microphone bias generator, allowing the microphone to interface with passive resistors and capacitors.

4.16.4 Microphone Input

The BK7252N provides a microphone input. The microphone signals can be amplified with the microphone input amplifier over a 0 to 32 dB gain range with a 2 dB step size.

4.16.5 Line In Input

The BK7252N provides a line in input. The line in signals can be amplified with the input amplifier over a 0 to 6 dB gain range with a 2 dB step size. The digitized line in signals can be further processed with the four-band equalizer prior to digital-to-analog conversion.

4.16.6 Audio Output

The BK7252N provides a high-fidelity mono audio output capable of driving a 16 Ω speaker with load capacitance up to 30 pF.

4.17 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 10-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC has the following features:

- Programmable sample rate from 14.5 kHz to 928.6 kHz
- 10-bit resolution
- Up to seven external analog input channels: ADC1/2/3/4/5/6/7
- Four internal dedicated channels:
  - VBAT monitoring channel (VBAT/3), connected to ADC0
  - TSSIO, connected to ADC8
  - Internal temperature sensor (TEMP), connected to ADC9
  - Internal debug channel, connected to ADC10
- Conversion modes:
  - One-shot mode
  - Software control mode
  - Continuous mode

4.18 Timer Groups (TIMG)

The BK7252N includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

4.19 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect and recover from failures or malfunctions. It triggers a reset on expiry of a specified time period.

The watchdog timer runs on the 32 kHz LPO_CLK clock and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

4.20 Real-time Counter (RTC)

The real-time counter (RTC) module features a 64-bit counter and a tick event generator. The RTC runs on the 32 kHz LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

4.21 IrDA Interface (IrDA)

The BK7252N embeds a hardware IrDA interface that supports waveform analysis and waveform generation. It monitors the start of infrared signals, records the sequence of infrared waveforms, stores the waveforms in the RX FIFO for software analysis, and writes the waveforms to be sent to the TX FIFO when sending, thereby enabling the analysis and transmission of any infrared protocol.

The IrDA has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

4.22 Temperature Sensor

The BK7252N integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read from the AUX ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

4.23 True Random Number Generator (TRNG)

The random number generator module generates true, nondeterministic random numbers based on thermal noise for the purpose of creating keys, initialization vectors, and nonces needed for cryptographic operations.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VCCBAT	Chip power supply voltage	-0.3	4.5	V
VCCUSB	USB power supply voltage	-0.3	6.0	V
VIO	IO LDO output voltage	-0.3	3.8	V
VCCPA	Supply voltage for PA	-0.3	3.8	V
VCCPAD	Supply voltage for PA driver	-0.3	3.8	V
VCCIF	Supply voltage for IF	-0.3	3.8	V
VCCRXFE	Supply voltage for RX	-0.3	3.8	V
VCCPLL	Supply voltage for RF PLL	-0.3	3.8	V
VDDRAM	Supply voltage for PSRAM	-0.3	3.8	V
VDDAON	AON LDO output voltage	-0.3	1.1	V
VDDDIG	Digital LDO output voltage	-0.3	1.1	V
VDDAUD	Audio LDO output voltage	-0.3	2.0	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	°C

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001	-	±2000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002	-	±500	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.(1)	Typ.	Max.	Unit
VCCBAT(2)	Chip power supply voltage	2.7	-	4.35	V
VCCBAT slew rate	-	300	-	-	mV/ms
VCCUSB	USB power supply voltage	4.3	5.0	5.5	V
VIO	IO LDO output voltage	2.8	-	3.5	V
VCCPA(2)	Supply voltage for PA	2.8	-	3.5	V
VCCPAD(2)	Supply voltage for PA driver	2.8	-	3.5	V
VCCIF	Supply voltage for IF	2.8	-	3.5	V
VCCRXFE	Supply voltage for RX	2.8	-	3.5	V
VCCPLL	Supply voltage for RF PLL	2.8	-	3.5	V
VDDRAM	Supply voltage for PSRAM	2.8	-	3.5	V
VDDAON	AON LDO output voltage	0.5	0.9	1.0	V
VDDDIG	Digital LDO output voltage	0.5	0.9	1.0	V
VDDAUD	Audio LDO output voltage	1.6	1.7	1.9	V
MICBIAS	Microphone bias output voltage	1.8	-	2.4	V
T_{OPR}	Operating temperature range	-40	-	85	°C

(1) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. Care must be taken when operating at the minimum specified voltage.

(2) To ensure WLAN performance, the ripple on the supply must be less than Vpp = 100 mV.

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VIO	-	VIO + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VIO	V
VOH	High-level output voltage	-	0.8 VIO	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VIO	V
I_{DRV}	I/O output drive strength	-	5	-	20	mA
R_{PU}	Weak pull-up resistor	-	-	48	-	kΩ

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PD}	Weak pull-down resistor	-	-	48	-	kΩ

5.5 Battery Charger

Parameter	Description	Min.	Typ.	Max.	Unit
VCCUSB	Charger input voltage	4.3	5.0	5.5	V
$I_{Trickle}$	Percentage of trickle charging current relative to fast charging current	-	10	20	%
I_{Fast}	Fast charging current	1.5	-	200	mA
V_{End} (calibrated)	VCCBAT voltage after charging is complete	-	4.2	-	V

5.6 IO LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO output voltage	2.8	3.3	3.5	V
Load current	-	-	-	500	mA

5.7 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital LDO output voltage	0.5	0.9	1.0	V
Load current	-	-	-	50	mA

5.8 AON LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAON	AON LDO output voltage	0.5	0.9	1.0	V
Load current	-	-	-	50	mA

5.9 Audio LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAUD	Audio LDO output voltage	1.6	1.7	1.9	V
Load current	-	-	-	5	mA

5.10 26 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	26	-	MHz
ΔF/F0	Frequency tolerance	25 °C	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 °C crystal	-20	-	+20	ppm
		-30 to 85 °C crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7.3	9	pF
TS	Trim sensitivity	-40 to 105 °C crystal	-	32	-	ppm/pF
		-30 to 85 °C crystal	-	17	-	ppm/pF

5.11 Current Consumption

Measured with T = 25 °C, VCCBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11b: 11 Mbps DSSS	-	42	-	mA
	11g: 54 Mbps OFDM	-	43	-	mA
	11n: MCS7, HT20	-	43	-	mA
TX current	11b: 11 Mbps DSSS @ 17 dBm	-	330	-	mA
	11g: 54 Mbps OFDM @ 15 dBm	-	280	-	mA
	11n: MCS7, HT20 @ 14 dBm	-	280	-	mA
Sleep Mode					
Sleep	-	-	90	-	μA

Parameter	Condition	Min.	Typ.	Max.	Unit
Deep sleep	-	-	16	-	μA
Shutdown Mode					
Shutdown	-	-	1	-	μA

5.12 WLAN RF Characteristics

5.12.1 WLAN Receiver Characteristics

Measured with T = 25 °C, VCCBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	-	-98	-	dBm
	2 Mbps DSSS	-	-94	-	dBm
	5.5 Mbps DSSS	-	-93	-	dBm
	11 Mbps DSSS	-	-90	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM	-	-91	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-76	-	dBm
Sensitivity - IEEE 802.11n (10% PER for 4096 octet PSDU)	HT20, MCS0	-	-89	-	dBm
	HT20, MCS1	-	-86	-	dBm
	HT20, MCS2	-	-84	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
	HT20, MCS3		-	-82	-	dBm
	HT20, MCS4		-	-78	-	dBm
	HT20, MCS5		-	-75	-	dBm
	HT20, MCS6		-	-73	-	dBm
	HT20, MCS7		-	-71	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11g: 6–54 Mbps (10% PER, 1000 octets)		-	-2	-	dBm
	11n: MCS0–7 (10% PER, 4096 octets)		-	-2	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	39	-	dB
	2 Mbps DSSS	-74 dBm	-	40	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	39	-	dB
	11 Mbps DSSS	-70 dBm	-	38	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g (10% PER for 1000 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	42	-	dB
	54 Mbps OFDM	-62 dBm	-	27	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	-	40	-	dB
	HT20, MCS7	-61 dBm	-	22	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
Spurious Emissions					
Spurious emissions	< 1 GHz	-	-	-60	dBm
	> 1 GHz	-	-	-50	dBm

5.12.2 WLAN Transmitter Characteristics

Measured with T = 25 °C, VCCBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX Power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	17.5	-	dBm
	11 Mbps DSSS	-	17	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	15	-	dBm
	54 Mbps OFDM	-	14	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	14	-	dBm
	HT20, MCS7	-	13	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-	-60	dBm
	> 1 GHz	-	-	-43	dBm

5.13 Bluetooth LE RF Characteristics

5.13.1 Bluetooth LE Receiver Characteristics

Measured with T = 25 °C, VCCBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz

Parameter	Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-96	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	8	21	dB
C/I 1 MHz adjacent channel	-	-	2	15	dB
C/I -1 MHz adjacent channel	-	-	-3	15	dB
C/I 2 MHz adjacent channel	-	-	-20	-17	dB
C/I -2 MHz adjacent channel	-	-	-31	-17	dB
C/I 3 MHz adjacent channel	-	-	-25	-18	dB
C/I -3 MHz adjacent channel	-	-	-31	-27	dB
C/I > 3 MHz adjacent channel	-	-	-31	-27	dB
C/I < -3 MHz adjacent channel	-	-	-31	-27	dB
Out-of-band blocking	30–2000 MHz	-30	-	-	dBm
	2003–2399 MHz	-35	-	-	dBm
	2484–2997 MHz	-35	-	-	dBm
	3000 MHz–12.75 GHz	-30	-	-	dBm
Intermodulation	-	-	-	-40	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-94	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	9	21	dB
C/I 2 MHz adjacent channel	-	-	2	15	dB
C/I -2 MHz adjacent channel	-	-	-3	15	dB
C/I 4 MHz adjacent channel	-	-	-20	-17	dB
C/I -4 MHz adjacent channel	-	-	-31	-17	dB
C/I 6 MHz adjacent channel	-	-	-28	-27	dB
C/I -6 MHz adjacent channel	-	-	-32	-27	dB
C/I > 6 MHz adjacent channel	-	-	-32	-27	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I < -6 MHz adjacent channel	-	-	-32	-27	dB
Out-of-band blocking	30–2000 MHz	-30	-	-	dBm
	2003–2399 MHz	-35	-	-	dBm
	2484–2997 MHz	-35	-	-	dBm
	3000 MHz–12.75 GHz	-30	-	-	dBm
Intermodulation	-	-	-	-50	dBm

5.13.2 Bluetooth LE Transmitter Characteristics

Measured with T = 25 °C, VCCBAT = 3.3 V unless otherwise stated.

Parameter		Condition	Min.	Typ.	Max.	Unit
General						
Frequency range		-	2402	-	2480	MHz
TX power		-	4	6	8	dBm
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-40	-20	dBm
	±3 MHz offset	-	-	-46	-30	dBm
	>±3 MHz offset	-	-	-47	-30	dBm
Modulation characteristics	Δf1avg	-	225	259	275	kHz
	Δf2max	-	185	250	-	kHz
	Δf2avg/Δf1avg	-	0.8	0.92	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	6	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	3	50	kHz
	$\|f_1 - f_0\|$	-	-	2	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2	20	kHz/50 μs
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	-28	-20	dBm
	±5 MHz offset	-	-	-44	-20	dBm

Parameter		Condition	Min.	Typ.	Max.	Unit
	>±5 MHz offset	-	-	-48	-30	dBm
Modulation characteristics	Δf1avg	-	450	518	550	kHz
	Δf2max	-	370	507	-	kHz
	Δf2avg/Δf1avg	-	0.8	0.94	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	10	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	3	50	kHz
	$\|f_1 - f_0\|$	-	-	2	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2	20	kHz/50 μs

5.14 Audio Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
DAC differential output	With 600 Ω load	-	1	-	Vrms
	With 16 Ω load	-	0.8	-	Vrms
DAC differential output THD	With 0.7 Vrms @ 600 Ω load	-	-	-80	dB
	With 0.65 Vrms @ 16 Ω load	-	-	-80	dB
DAC output SNR	1 kHz sine wave	-	104	-	dB
DAC sampling rate	-	8	-	48	kHz
ADC SNR	1 kHz sine wave	-	92	-	dB
ADC sampling rate	-	8	-	48	kHz

5.15 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	0.2	-	13	MHz
Conversion time	-	-	14	-	Cycle
V_{REF}	Internal	0.8	1.8	-	V
	External	-	VIO/2	-	V

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range	-	0	-	V_{REF}*2	V
Input impedance	-	100	-	-	MΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-1	-	0.5	LSB
INL	-	-2	-	2	LSB
ENOB	-	-	9.2	-	Bit
SNDR	-	-	57	-	dB
SFDR	-	-	61.4	-	dB
$T_{STARTUP}$	-	-	5	-	μs
Current consumption	-	-	200	-	μA

6. Package Information

6.1 QFN68 8 x 8 mm Package

Figure 6-1 QFN68 8 x 8 mm Package Outline

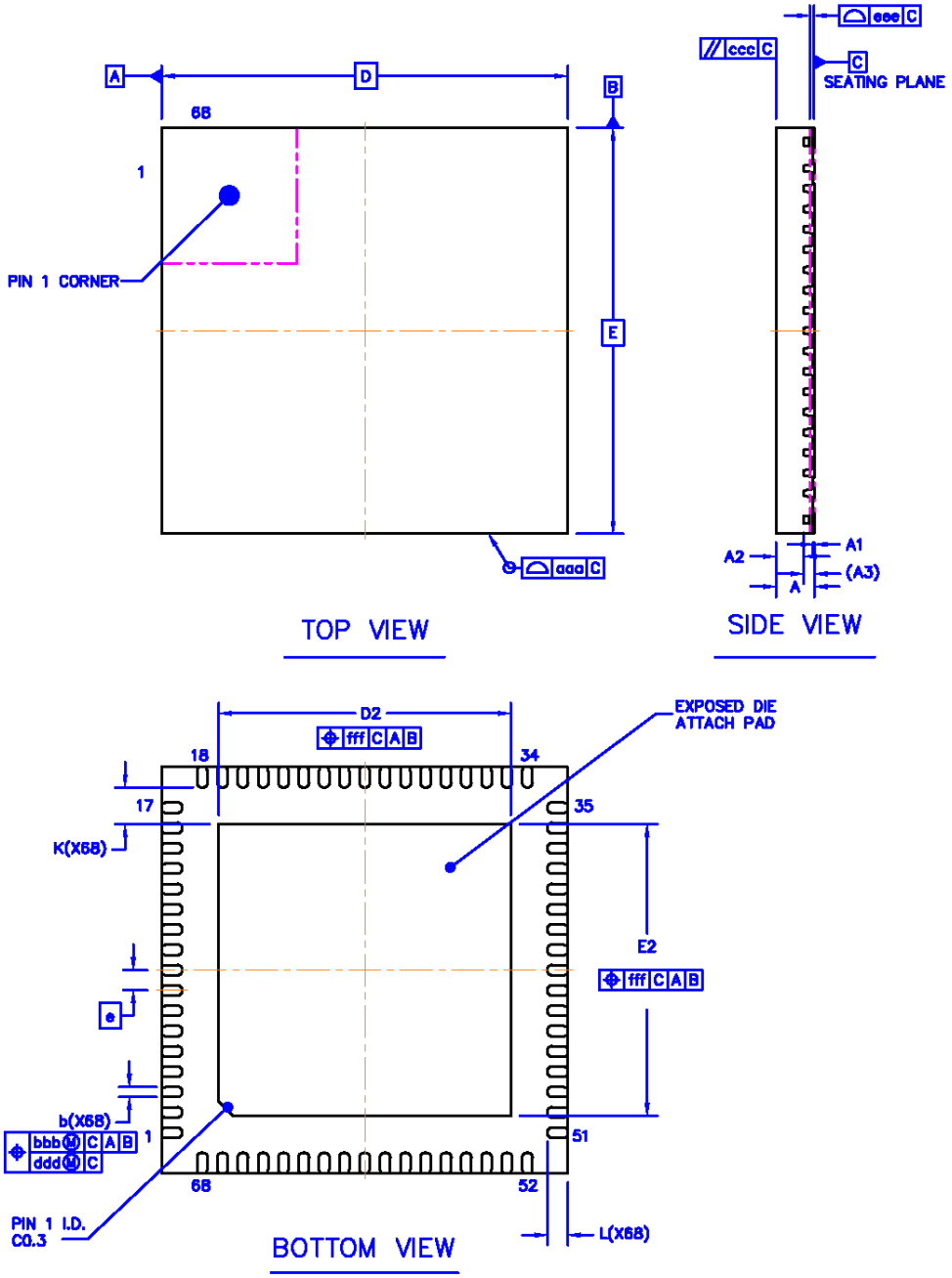


Table 6-1 QFN68 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
D2	5.65	5.75	5.85
E2	5.65	5.75	5.85
L	0.30	0.40	0.50
K	0.725 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

6.2 QFN48 6 x 6 mm Package

Figure 6-2 QFN48 6 x 6 mm Package Outline

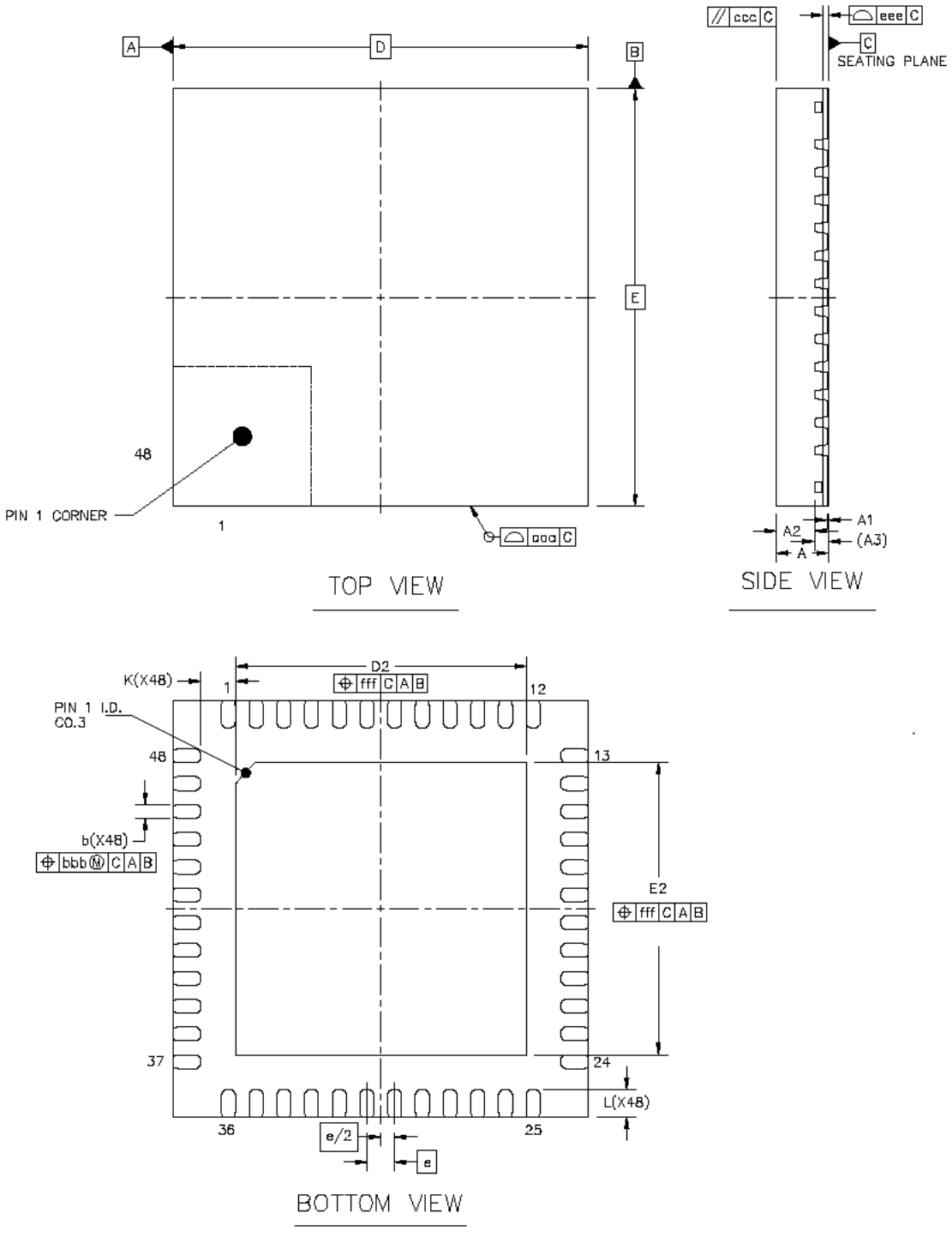


Table 6-2 QFN48 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
D2	4.10	4.20	4.30
E2	4.10	4.20	4.30
L	0.30	0.40	0.50
K	0.50 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
fff	0.10		

6.3 QFN40 5 x 5 mm Package

Figure 6-3 QFN40 5 x 5 mm Package Outline

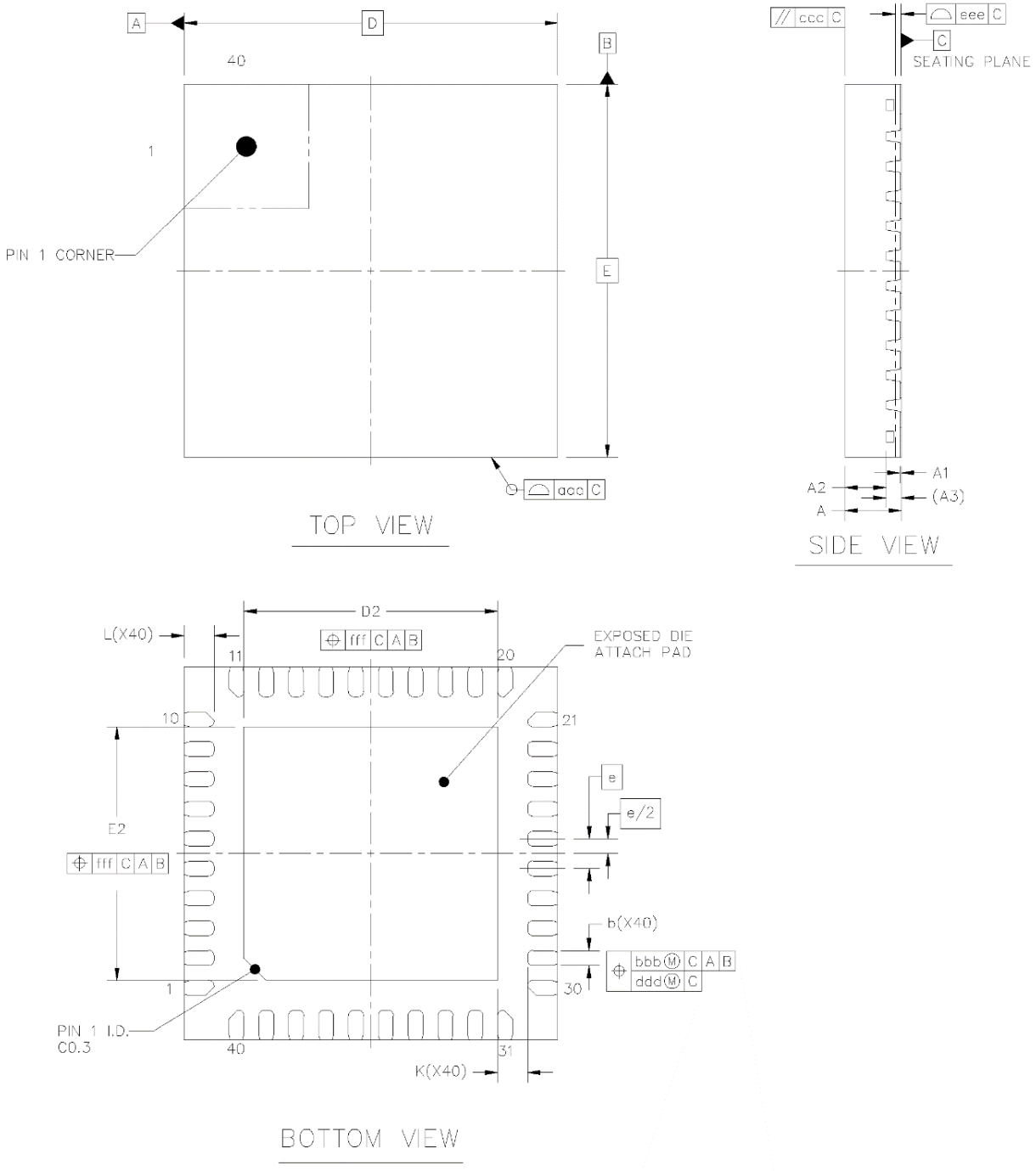
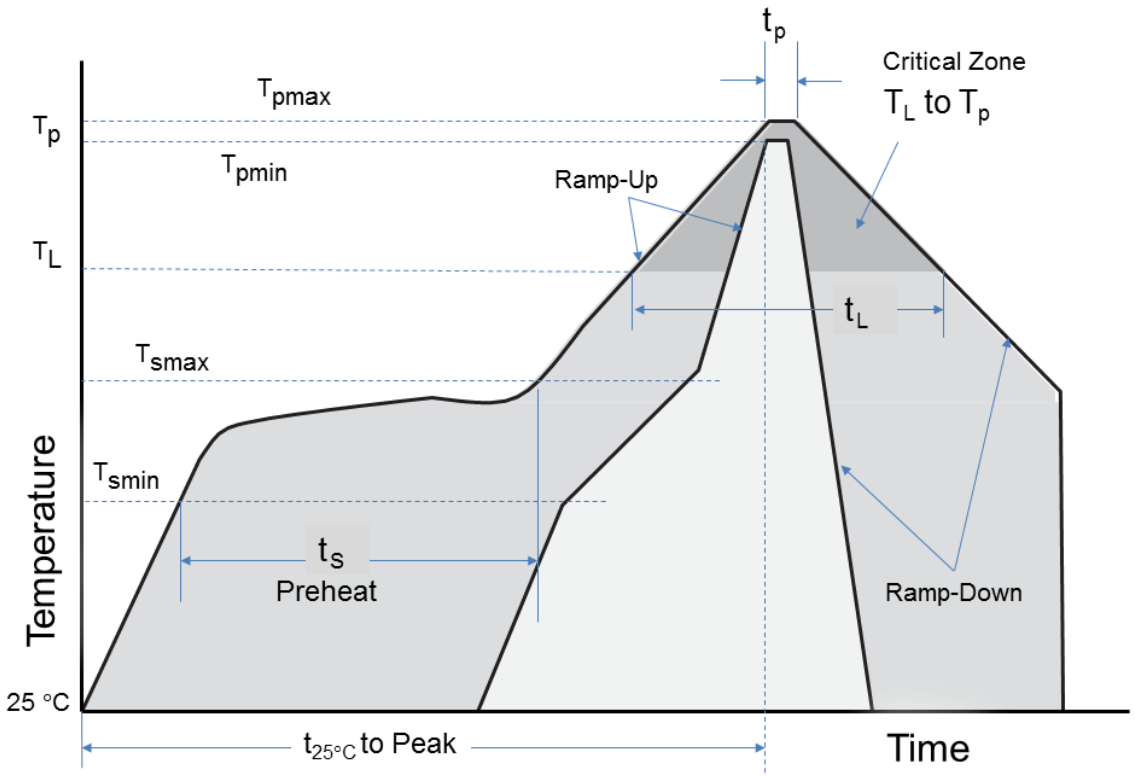


Table 6-3 QFN40 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
L	0.30	0.40	0.50
K	0.40 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 °C/s max.
Preheat	Temperature min. (T_{smin})	150 °C
	Temperature max. (T_{smax})	200 °C
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 °C
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 °C
Time within 5 °C of actual peak temperature (t_p)		20 s to 40 s
Ramp-down rate		6 °C/s max.

Profile Feature	Specification
Time 25 °C to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Ordering Code Scheme

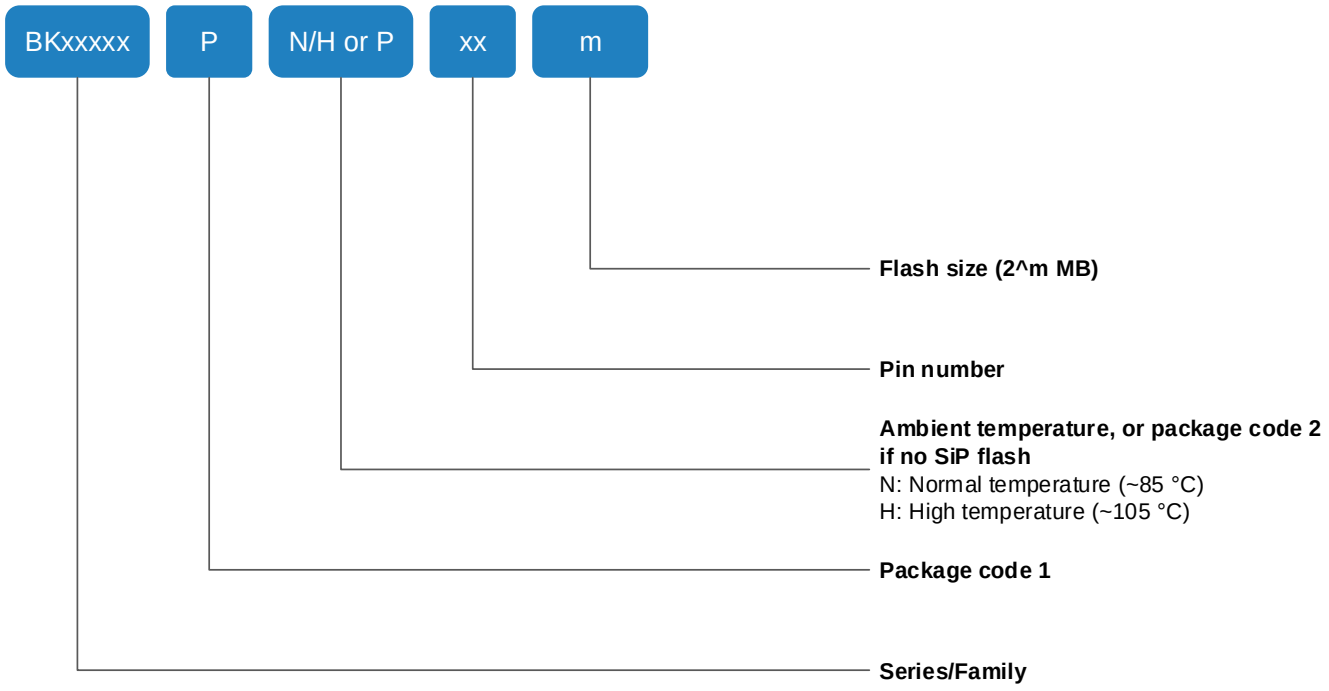


Table 8-1 Ordering Information

Ordering Code	Package	SiP(1) Flash	Packing	Minimum Ordering Qty (MOQ)(2)
BK7252NQN681	8 mm x 8 mm QFN68	2 MB	Tape and Reel	3000
BK7252NQN682	8 mm x 8 mm QFN68	4 MB	Tape and Reel	3000
BK7252NQN481	6 mm x 6 mm QFN48	2 MB	Tape and Reel	3000
BK7252NQN482	6 mm x 6 mm QFN48	4 MB	Tape and Reel	3000
BK7252NQN400	5 mm x 5 mm QFN40	1 MB	Tape and Reel	3000
BK7252NQN401	5 mm x 5 mm QFN40	2 MB	Tape and Reel	3000

(1) A system in a package (SiP) refers to flash enclosed in the package.

(2) The MOQ for customized or exclusive ordering codes is one wafer lot. Please consult your sales representative for the exact quantity.

Revision History

Version	Date	Description
1.0	2025/6/11	Initial release

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Beken Corporation

Building 41, 1387 Zhangdong Rd

Shanghai 201203

China

http://www.bekencorp.com